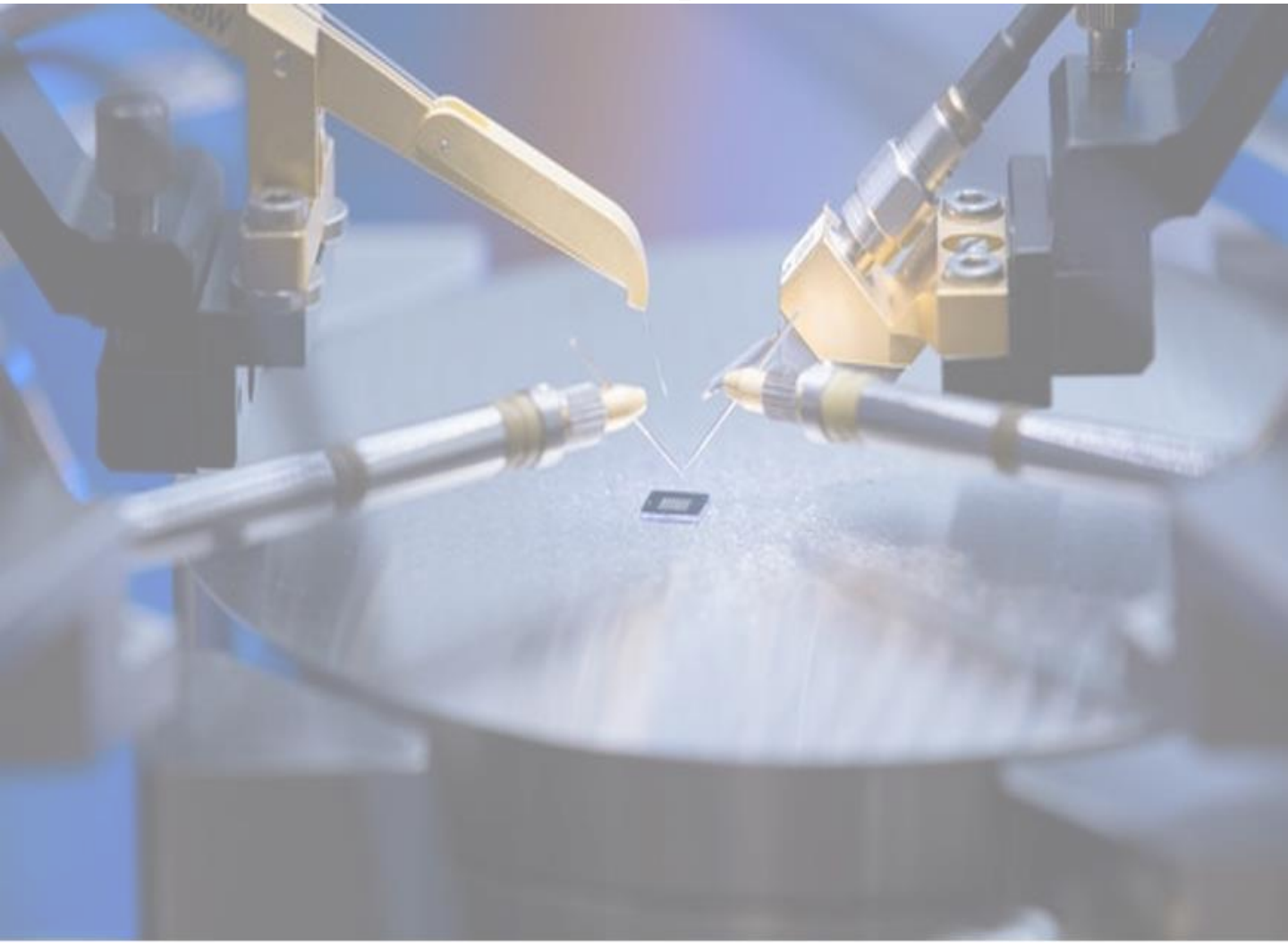
CS Hub

Future Compound Semiconductor Manufacturing Hub

Annual Report 2021



Establishing the UK as the primary global CS research and manufacturing hub

Grant number
EP/P006973/1

UKRI Engineering and Physical Sciences Research Council

https://compoundsemiconductorhub.org

CONTENTS

WELCOME MESSAGE

The last year has had terrible consequences for many and been a challenging one for the CS Hub. However, there have also been new opportunities to collaborate with our academic and industrial partners and to work towards our long term goal of establishing the UK as the global centre for CS research and manufacturing.

The Hub started as a partnership between Cardiff University, the University of Manchester, the University of Sheffield, University College London and 24 original industrial backers. Through feasibility and follow on funding we have added contributors from the Universities of Bath, Bristol, Cambridge, Lancaster, Oxford, Strathclyde, Swansea and Warwick and now actively engage with over 30 industrial partners and other organisations including other Manufacturing Hubs and centres of critical mass such as the EPSRC National Epitaxy Facility.

We are addressing long term research challenges and in the past year have continued to make progress in the scale-up of manufacturing of compound semiconductor components, in epitaxially manufacturing compound semiconductor electronic and photonic structures on silicon including novel memory elements, in magnetic imaging systems for non-destructive testing and in display and communication technology based on GaN micro-LEDs and integrated HEMTs.

Our partner activity, the EPSRC Centre for Doctoral Training (CDT) in Compound Semiconductor Manufacturing is in its second year, with currently a total of 21 students and a further 14 expected in October 2021. We are continuing to receive strong support from industry, with three quarters of the PhD projects being jointly cash-funded and all receiving external in-kind support. The CDT also leads on providing a series of training sessions given by our industry partners.

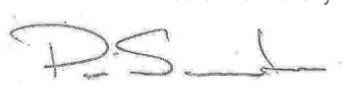
During lockdown the Hub has provided online training sessions given by academics and postdoctoral researchers to spread expertise and good practice across the Hub. Due to their success we expect to continue these as we hopefully move to more normal working, to supplement our in-person training.

We have continued to work closely with our industrial partners to shape our research. Last year saw the Hub carrying out its first online survey of industrial partners to gain a better understanding of their research and skills challenges and needs. Following on from this and subsequent in-depth discussion we recently hosted an online workshop with the CSA Catapult and a number of industrial partners which explored the challenges and added value of advanced (packaging) semiconductor integration.

In March 2021 we welcomed friends to the 34th Semiconductor and Integrated OptoElectronics (SIOE) Conference. We were able to successfully translate the conference into an exciting online three day programme with over 260 delegates attending. The programme included live talks on a wide range of topics from invited international speakers and a panel session exploring the future of the integration of Electronics and Photonics.

Finally, I would like to thank all of our colleagues for coming together during this difficult time. The even closer working and partnership across a geographically diverse grouping and exemplified by the technical and personal support for others during our regular zoom meetings has kept us all going.

Prof Peter Smowton
CS Hub Director,
Cardiff University



INTRODUCTION

EPSRCs vision for their critical mass investments is to support UK manufacturing industries by supporting the commercialisation of early stage research opportunities in emerging areas, through a network of Future Manufacturing Research Hubs.

Each Hub has a programme of innovative research in the engineering and physical sciences, related to the challenges in commercialising early stage research. A key characteristic of the Hub model is that the research is driven by the long-term research challenges of users. User collaboration is therefore an essential aspect for these Hubs.

The vision of The Future Compound Semiconductor Manufacturing Hub (CS Hub) is to establish the UK as the primary global research and manufacturing hub for Compound Semiconductor (CS) Technologies by combining and connecting the UK research excellence in CS, with the very best translational facilities and the new Compound Semiconductor Catapult to support the UK CS industry and UK industry users of CS. The combined activity provides a path from enabling fundamental research through wafer, device and integrated chip manufacturing research into prototyping, reliability testing and system qualification.

The CS Hub has 3 key outcomes:

- To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
- To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
- To generate novel integrated functionality such as sensing, data processing and communication.

The Hub forms an integral part of the CS Cluster based in South Wales, and also serves and supports CS manufacturing and applications related industry throughout the UK. The CS Cluster forms a complete manufacturing chain from Technology Research Level (TRL) 1 to 9 and currently comprises 9 collaborating partners. The Hub makes use of the world leading facilities and expertise at the Institute for Compound Semiconductors (ICS, Cardiff University) and feeds the higher TRL 4+ activity at the Compound Semiconductor Centre (CSC) which links to the UK manufacturing industry and the Compound Semiconductor Catapult. The Hub is resourced to research and develop new manufacturing processes, leveraging existing capital investment and completing the Welsh and UK Government strategy to generate a major UK CS Cluster.

Compound semiconductors are essential for the development of:

- 5G
- energy efficient lighting
- smart devices
- electric vehicles
- imaging techniques

Compound semiconductors are vital to development of technologies supporting:

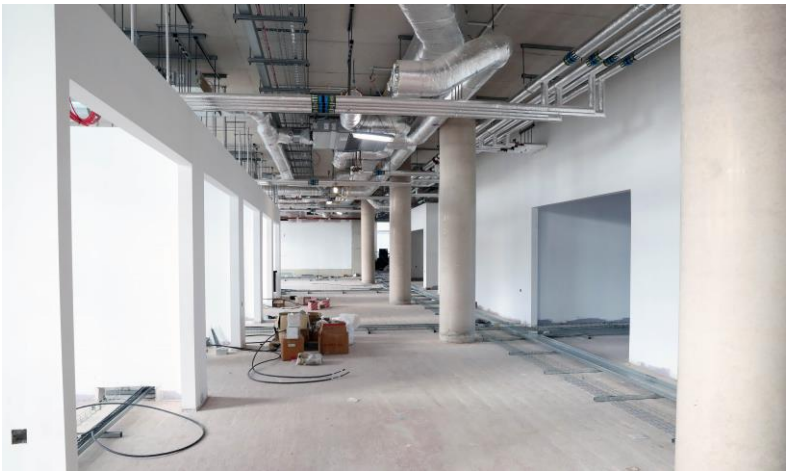
- a connected world
- health
- security
- the environment.

The Hub will:

- position the UK at the centre of CS manufacturing research
- support & promote CS research and systems research in all associated fields
- apply the manufacturing disciplines and approaches used with Silicon semiconductors
- combine CS with Silicon to generate the required increase in CS manufacture.

Translational Research Hub

The Translational Research Hub (TRH) at Cardiff University is due to open in 2022 and will house the Institute for Compound Semiconductors.



Construction is underway inside the TRH. The University challenged designers HOK to create an environment that both inspired the imagination, fostered the health and wellbeing of building occupants and served as a showcase space for attracting and retaining top-tier students and researchers.

A central atrium serves as a daylight-filled welcome area and event space where visitors can peer into labs to see the ground-breaking research underway. A canopy-covered entrance plaza, exterior rain garden and a green roof over the atrium offer additional space outside the building.

HUB STRUCTURE

Our Hub of CS research activity and operational headquarters is located at Cardiff University, led by Hub Director, Professor Peter Smowton. This central entity interacts highly with spoke including universities: University of Manchester, University of Sheffield and University College London, as well as a large number of industrial partners and collaborators.

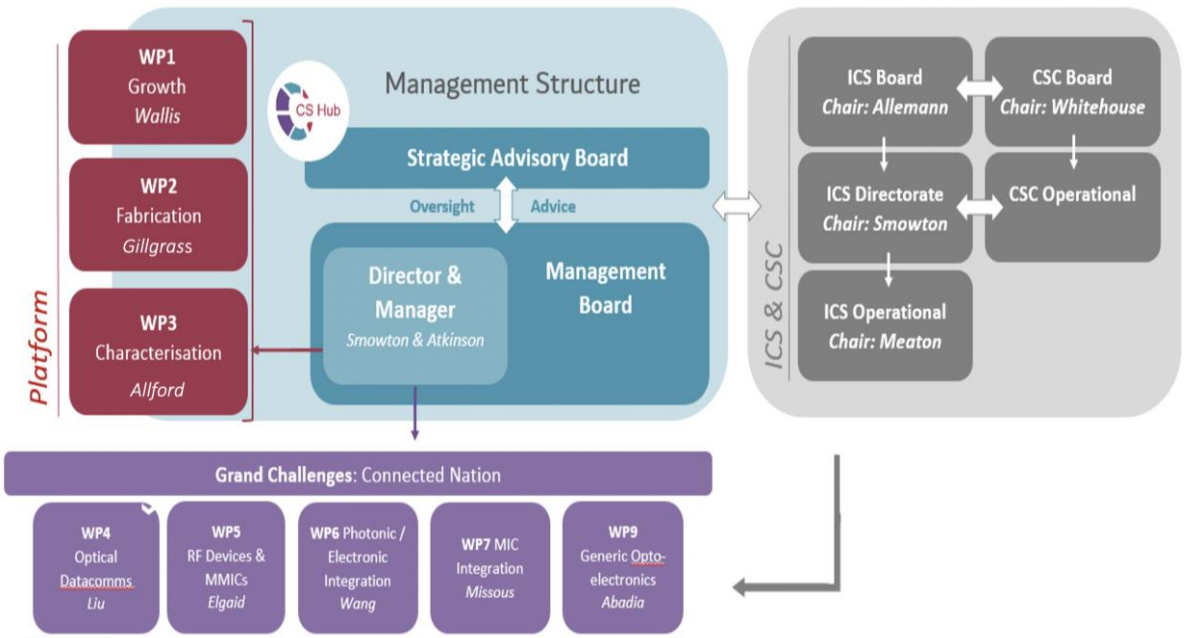
The Hub structure includes a Management Board and Strategic Advisory Board, as well as support structures for each of the Hub's 8 work packages.

Management Board

The Hub Management Board (MB) is responsible for the strategic and operational management of the Hub, including making decisions on the allocation of funding. The MB is comprised of a number of senior Hub members who are able to represent the research interests of the Hub. All members meet quarterly to discuss and plan the research of the CS Hub, in addition to other areas the MB is responsible for, including ED&I and learning and development. The MB reports to the Hub Strategic Advisory Board (SAB) every 6 months.

Strategic Advisory Board

The SAB provide guidance to the Hub MB via a biannual meeting. The Board includes world leading research and industry experts in the field of compound semiconductors. Strategic Advisory Board meetings provide an opportunity for Hub members to receive guidance and direction from impartial, highly experienced and knowledgeable individuals.



The CS Hub Management Structure. The Director is advised by a Management and Strategic Advisory Board.

CS Hub Management Board members

Prof Huiyun Liu	University College London
Dr. Wyn Meredith	Compound Semiconductor Centre
Prof. Mo Missous	University of Manchester
Prof. Peter Smowton	Cardiff University
Prof. Paul Tasker	Cardiff University
Prof. Tao Wang	University of Sheffield

Strategic Advisory Board members

Dr. John Bagshaw	Independent Technology Consultant
Dr. Maria Ana Cataluna	Heriot-Watt university
Dr. Ivona Mitrovic	University of Liverpool
Prof. Richard Penty	Cambridge University
Prof. Dominique Schreurs	KU Leuven
Dr. Andy Sellars	CSA Catapult
Dr. Carol Trager-Cowan	University of Strathclyde

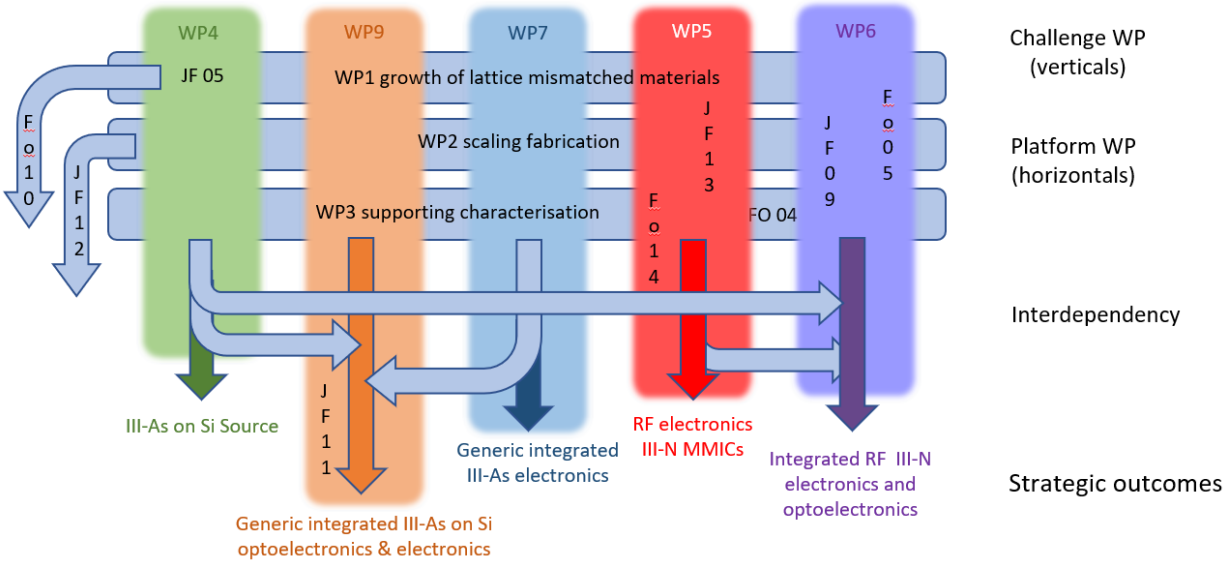
Hub Work Package Leads

Prof. David Wallis	Cardiff University	WP1 Lead
Dr. Sara-Jayne Gillgrass	Cardiff University	WP2 Lead
Dr. Craig Allford	Cardiff University	WP3 Lead
Prof. Huiyun Liu	University College London	WP4 Lead
Prof. Khaled Elgaid	Cardiff University	WP5 Lead
Prof. Tao Wang	University of Sheffield	WP6 Lead
Prof. Mo Missous	University of Manchester	WP7 Lead
Dr. Nicolas Abadia	Cardiff University	WP9 Lead

Membership of the CS Hub management structures is shown in the tables above. The Hub is governed by a Management Board made up of senior members of the Hub team across the four original academic partner institutions.

The Strategic Advisory Board is made up of experts from academia and industry who are well equipped to advise the Hub on research direction, identifying commercially valuable research and advising on impact paths. Our work package and grand challenge leads direct and coordinate the research of the Hub.

HUB STRUCTURE



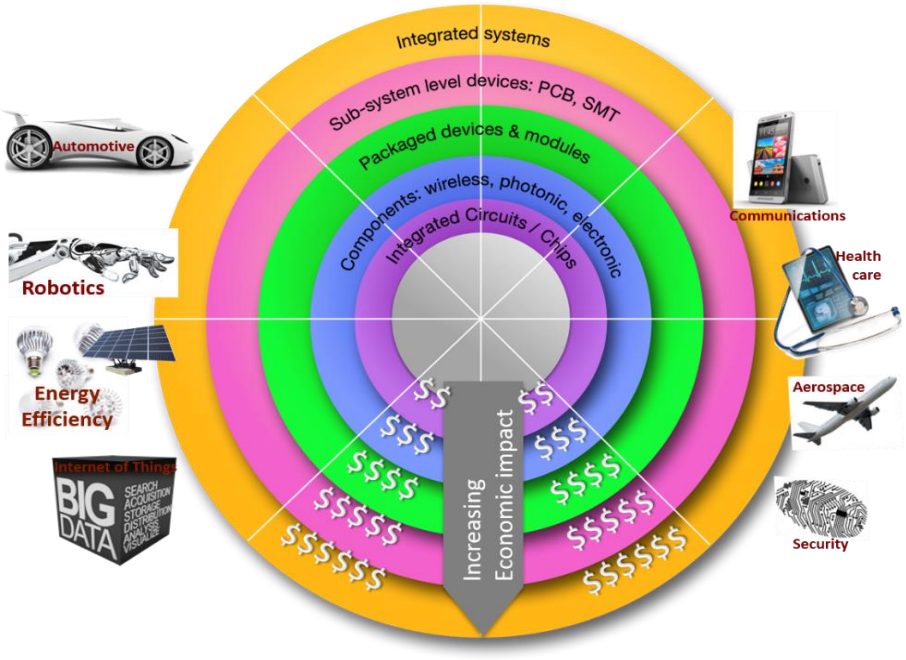
Work Package (WP) structure of the CS Hub. Grand challenge WPs are supported by 3 "platform" areas and have been made more effective by the addition of a number of feasibility (JF) and follow-on (FO) activities from other universities, together focussed on achieving the strategic outcomes.

Next generation technologies will only be achieved with a huge increase in compound semiconductor manufacture.

Compound semiconductor materials are a Key Enabling Technology at the heart of modern society.

Key Outcomes:

- To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
- To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
- To generate novel integrated functionality such as sensing, data processing and communication.

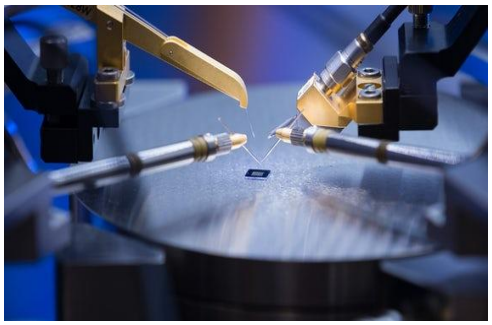


The diagram indicates the likely impact areas of technology developed via the CS Hub and emphasises the added value at each stage enabled by the CS technology.

CS Cluster developments

The Hub remains an active and founding member of the CS Cluster in South Wales. CSconnected is the formal gateway to the Cluster which represents organisations directly associated with research, development, innovation and manufacturing of compound semiconductor related technologies, as well as organisations along the supply chains whose products and services are enabled by compound semiconductors.

Other members of CSconnected include core partners, the Institute for Compound Semiconductors (ICS, Cardiff University), the Compound Semiconductor Centre Ltd (CSC), the Compound Semiconductor Applications Catapult and the Centre for Integrative Semiconductor Materials (CISM, Swansea University). These are joined by business partners IQE plc, SPTS, Microchip, and Newport Wafer Fab. Together we complete the supply chain for brining new CS discoveries to market. The development of the CSconnected brings us closer to achieving our mission of "establishing the UK as the primary global CS research and manufacturing hub"



CCR City Deal

Significant investment (£37.9m) from the Cardiff Capital Region (CCR) City Deal has enabled Cluster members, IQE plc to develop a new high-tech facility in Newport. This has generated employment for a number of highly skilled engineers and technicians.

Image adapted from CS Catapult material. The CS Hub covers TRL levels 1 to 4 and works together with ICS, the CS Centre and the CS Catapult, together with several other partners, to form the CS Cluster.

CS Applications Catapult

In 2018, the Compound Semiconductor Applications Catapult opened an impressive Innovation Centre, which is co-located with IQE in Newport, South Wales. The state-of-the-art building houses a design studio, laboratories and test facilities for power electronics, photonics and RF, supported by simulation and modelling tools and an advanced packaging facility. CSA Catapult currently employs 87 highly qualified staff, with many educated to PhD level. The organisation is focused on bringing compound semiconductor applications to life in three key areas: the road to Net Zero, future telecoms and intelligent sensing, and helps companies develop new products using compound semiconductors. They are currently working on projects valued at £142m with 27 academic partners and 84 industrial partners.

CSA Catapult Innovation Centre, which is co-located with IQE in Newport, South Wales.

UKRI Strength in Places

CSconnected led a successful £42m bid to develop a CS powerhouse in South Wales. Government funding provided through UK Research and Innovation's flagship Strength in Places Fund will build a world-leading cluster of excellence in CS technologies – CSconnected - bringing economic investment and high quality jobs to the region.

The winning consortium connects Cardiff University, Swansea University, a range of key regional industrial partners including IQE, SPTS, Newport Wafer Fab (NWF), Cardiff Capital Region City Deal, Welsh Government and UK Government's Compound Semiconductor Applications Catapult. The Strength in Places funding will help CSconnected bring together combined public and private sector investment to build the CSconnected and wider supply chain, grow new companies and create high value jobs, innovation programmes and investment in skills that can help the region recover its strength after the COVID-19 pandemic.

The project will create a talent pipeline that creates highly skilled, well paid jobs, bringing social and economic benefits to South Wales and includes developing a design centre and module manufacturing in the region, as well as developing the next generation of semiconductor wafer fabrication toolsets with enhanced production capacity, novelty and efficiency: facilitating the development of enhanced wafer processing techniques and equipment.

Societal

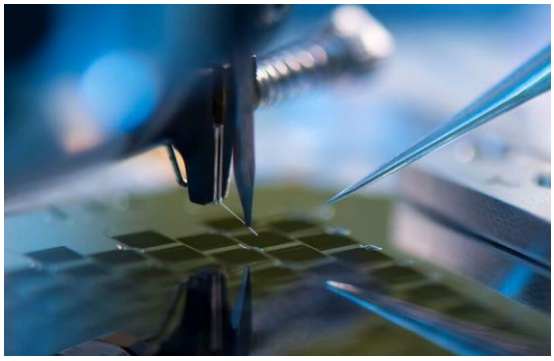
Compound Semiconductor materials are a Key Enabling Technology underpinning the operation of the internet and enabling emerging megatrends such as smart phone usage, satellite communications/GPS, direct broadcast TV, energy efficient lighting, efficient solar power generation, advanced healthcare and ground breaking biotechnology. Simply put these technologies support our connected world and the future health of the planet.

Knowledge Dissemination

We are active in dissemination of knowledge via conferences such as UK Semiconductors and Photonics West, the latter providing an excellent mix of science and commercial activity. We will publish in open access peer reviewed journals such as those from both the Nature and IEEE tables. Our aim remains to engage new partners and we hold workshops, use feasibility funding, actively canvas and make use of our existing partners and contacts, relevant KTNs, the Welsh Optoelectronics Forum and other appropriate bodies to connect as widely as possible.

Outreach

We hope to have increasing opportunities for face to face outreach activity over the coming year and work with our cluster partners to expand the Hub's outreach. More information is provided in the outreach section from page 36.



Skills Base

The cutting edge equipment operated as part of a manufacturing process offers an excellent training opportunity, inculcating a manufacturing mind set in a UK strategically relevant high technology field. We embed technological excellence and the latest manufacturing approaches in UK industry. PDRAs and students participate in high level meetings with the commercial organisations and work alongside R&D staff from industry. There is also a direct economic impact via the provision of skilled workers to relevant companies.

Economic

Our vision is to ensure that the UK's research strength in compound semiconductors will be embedded in manufacturable approaches so the UK can commercially address the opportunities that compound semiconductors will provide. The global market for compound is expected to grow to 44.5 billion USD by 2027. Expanding commercial activity in the compound semiconductor sector will provide an important boost for the UK economy and maintain UK advanced manufacturing competitiveness. A good example of this is Cardiff headquartered IQE Plc, the global leader in supplying compound semiconductor materials (with turnover of 178m, 2020 results).

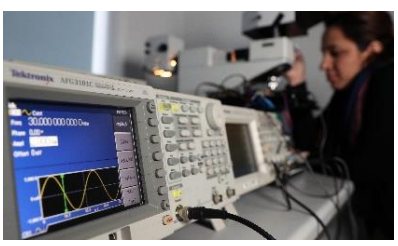
Our aim is to strengthen the relationship between academia and industry and this will be achieved by 1) changing the mind set of researchers to start from solutions that allow rapid translation to production by providing access to production scale and research tools that are functionally similar along with highly skilled support for the tools and processes; 2) Co-location of research and industry staff to maximise cross fertilisation of ideas, techniques and approach in an environment that supports interaction. The Hub together with staff from the Compound Semiconductor Centre will support SMEs through product prototyping, IP generation, skills development and training. They will help bid for external grants, coordinate partner forums, form networks and prepare roadmaps.

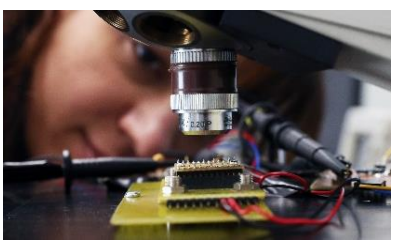
TRANSLATION

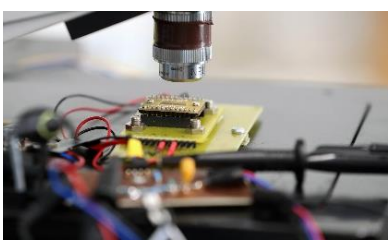
In 2014 the Sheffield led EPSRC III-V centre CS roadmap identified a concern that the UK CS community was missing an exploitation link to help provide a route to impact and exploitation. Many technological solutions work well in the research environment but fail to succeed commercially. The Hub directly addresses this issue, by working to change the academic community mind set, to inspire researchers, via training and environmental changes, so they begin with solutions that allow rapid translation.

The Hub is encouraging the co-location of research and industry staff to maximise interactions. Our research is specifically designed to produce intermediate outputs that can be used to demonstrate the potential for successful translation. In order to promote this activity across the wider UK community, the Hub had £1m to invest in new research projects (described in more detail in the feasibility study section of this report). We invested in a first round of 6 initial short-term projects, followed by 4 continuation studies and 5 new studies as a result of our joint feasibility 2019 call with other manufacturing hubs. Funded studies have a high probability of translatable manufacturable research, and are expected to cascade into subsequent larger studies with an emphasis on translating technology from research to industry. We recognise that SME engagement is a critical element in promoting rapid exploitation opportunities and interact with a number of these.

Future Compound Semiconductor Manufacturing Hub	Institute for Compound Semiconductors	Compound Semiconductor Centre	Compound Semiconductor Applications Catapult
CS Manufacturing Research	Facilities; Equipment; Services (skilled workers)	Develop and prototype CS materials	Accelerate the development of products using compound semiconductors
Enable high value & productivity in CS manufacturing	Scale Fabrication	Enable a wide range of applications	Market intelligence Consortia building Supply chain management Project management
Building on CS research	Product development to prototyping	Translate R&D to product & process innovation to high value large scale manufacturing	Design studio with simulation and modelling Power electronics lab Photonics lab RF/microwave lab Advanced packaging lab
Training; Outreach	Industrial collaboration		Knowledge Transfer Partnerships







Images show device development by a Hub PhD student, Cardiff University.

EXPLOITATION ROUTES DRIVING IMPACT 13

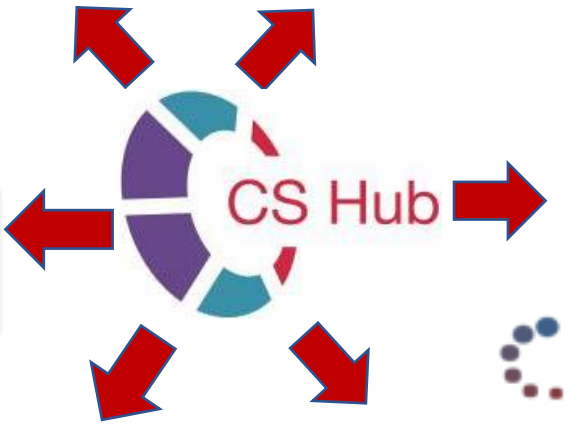
Translational funding

The Hub strives to connect its EPSRC research activity through e.g. Innovate UK funding to higher TRLs and commercial exploitation. As planned further translational funding with industry partners is driving this impact route. Since the start of the Hub several translational Innovate UK projects have begun, and industry partners have provided funding for studentships via either CASE awards or via cofunding with the EPSRC Centre for Doctoral Training in Compound Semiconductor Manufacturing. Technology developed in the Hub is also embedded in the Institute for Compound Semiconductors and the EPSRC National Epitaxy Facility, which are both open access facilities for UK academics and UK industry.

MAG-V : Enabling Volume Quantum Magnetometer Applications through Component Optimisation & System Miniaturisation. Innovate UK

Quantum Electro-Optic Detector Technology(QuEOD). Innovate UK

Strength in Places.
CSconnected UKRI



SLOGaN M4 – Short Loop Optimisation of Gallium Nitride Materials and Major Manufacturing Modules. Innovate UK

Kairos. Innovate UK

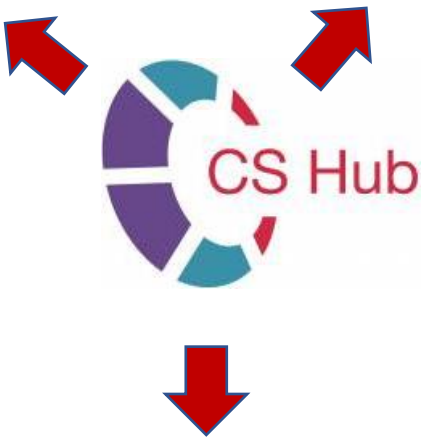
Cardiff University / Prifysgol Caerdydd — Institute for Compound Semiconductors — Sefydliad Lled-ddargludyddion Cyfansawdd

NATIONAL EPITAXY FACILITY

EXPLOITATION ROUTES DRIVING IMPACT

Qfoundry. Innovate UK

GaN on SiC RF. Smart Expertise



Studentships CASE, for example with:

IQE AIRBUS

EPSRC CDT in Compound Semiconductor Manufacturing

LEONARDO

SPTS A KLA Company

NEWPORT WAFER FAB

NPL National Physical Laboratory

IQE

qorvo all around you

Rockley PHOTONICS

LINWAVE TECHNOLOGY

CATAPULT Compound Semiconductor Applications

HUAWEI

Research and skills surveys

In order to understand the areas of Compound Semiconductor research of most interest to our industry partners and their skills challenges and needs, the Hub developed research and skills surveys. We shared the surveys with a range of new and existing industry partners to gather the best insights in these areas.

The insights gained helped us as part of a wider review of the Hub's research and supported our future planning. The surveys also helped us to understand the specific challenges industrial partners have faced as a result of Covid. The Hub Management Board and Strategic Advisory Board have used the surveys insights to further inform discussion on the Hub's strategic direction and the responses have also provided the basis for a series of more in-depth discussions with industry partners.

Packaging the future – connecting semiconductors to the consumer

The CS Hub and CSA Catapult recently hosted (May 2021) an interactive online workshop, exploring the challenges and added value of advanced (packaging) semiconductor integration. The aim of the event was to get packaging considered and included at an earlier stage during the device development phase, with researchers and industry partners discussing key challenges and solutions. The workshop was attended by over 30 academics and industry partners, with four presentations from the Hub on mature projects looking for routes to commercialisation and earlier stage issues around integrated circuits. Four industry partners subsequently presented on their capabilities, and this was followed by an engaging roundtable discussion with a wider set of academics and industry partners. The event provided a forum to discuss long established challenges and will foster further collaboration between the Hub and industry. Below are some quotes from industry partners who attended and presented at the event:

"It was an excellent opportunity to expose the breadth of packaging challenges and evolving solutions that need to be catalysed in UK".
Geoff Haynes: Business Development Manager at RAM Innovations Ltd.

"A really useful workshop highlighting the importance of, and a rallying call, to take packaging seriously from the start".
Glenn George: Managing Director at Bay Photonics ltd

"I thought the event was well organised and gave an interesting insight into the research being done, and how that can blend with the innovations in the UK packaging industry".
Matt Booker: Head of Sales – Assembly Services at ALTER TECHNOLOGY TÜV NORD UK Ltd

"I found it very informative to learn about technologies outside my immediate field, discuss the packaging challenges we all face and understand how our collective capabilities could address those".
Ross Wheeler | III-V IR Product Development Manager & Technical Authority | Space Imaging

COMMENTS FROM INDUSTRY PARTNERS 16

"SPTS manufacture plasma etch and deposition equipment for the semiconductor industry. As compound semiconductor applications take a more prominent role in providing solutions for future needs of society, we are excited to be a core partner in the CS Cluster. Bringing together academia, and research consortia enables us to be more effective at industry solving challenging problems in this exciting environment. Having the expertise and resources of the CS Hub so easily accessible has helped us to understand the technologies we work with to a much deeper level, and this ultimately helps us to serve our customers' and industry's needs better".

Huma Ashraf: Process Technology Manager, SPTS Technologies

SPTS
A KLA Company

"The wireless application technology development at The EPSRC Future Compound Semiconductor Manufacturing Hub (CS Hub) provides an important platform in developing an industry scale RF GaN on Si Technology for wireless applications and is closely linked with and complementing other Newport Wafer Fab manufacturing and RD&I Compound Semiconductor activities. Further, the RF GaN on Si activities within CS Hub will induce synergies and opportunities to other UK industry in the filed from wafer development to system level for commercial, industrial and defence applications".

Sam Evans: Director of TQ Engineering, Newport Wafer Fab

NEWPORT
WAFER FAB

Overview

Our partner activity, the EPSRC Centre for Doctoral Training (CDT) in Compound Semiconductor Manufacturing is in its second year, with 14 students joining us in October 2021 bringing total numbers to 21. A total of 65 students are expected over the five intakes of the current EPSRC funding.

EPSRC CDT in **Compound Semiconductor** Manufacturing

The CDT aims to develop PhD graduates with multidisciplinary skills, which will help to supply the staff needed to support the rapid growth of the world's first Compound Semiconductor Cluster. Our ambition is to change the face of CS research in the UK by training the new generation to understand how to facilitate the translation of research into production.

The CDT has a structured training programme in the first year, based on the MSc in Compound Semiconductor Physics or Electronics, delivered by Cardiff University which includes practical cleanroom training. Alongside the MSc modules, the cohort participate in research seminars offered by our partner universities, University of Manchester, University of Sheffield and UCL to broaden their understanding of key issues in CS research.

In the spring semester, alongside skills seminars, Manufacturing Method seminars are offered by our industrial partners, exposing students to topics in the manufacturing chain. During 2020-21, the topics were:

Advanced Semiconductor Manufacturing and Control: Statistical Methodologies and Management Systems: Sam Evans, Newport Wafer Fab

Commercial MMIC Design and Consultancy: Dr Robert Smith, PRFI

Design for Packaging: Dr William Doward, Alter Technology

Technology Development and the Route to Market: Dr Gareth Jones, LUX-TSI

Site Visit: Newport Wafer Fab

EPSRC CENTRE FOR DOCTORAL TRAINING (CDT) 18

Despite the restrictions due to COVDI-19, the seven students in our first cohort are progressing well on their PhDs and two presented their work at the SIOE (Semiconductor and Integrated Optoelectronics) Conference in March. Bogdan Raitu, co-funded by Rockley Photonics, gave a talk and won 'Best Oral Presentation' while Paradeisa O'Dowd Phanis, co-funded by Leonardo MW, presented a poster.

We have had strong support from our industry partners for co-funding of PhD projects. In Cohort 1, five of seven projects have industrial co-funding, while 11 of 14 projects selected by Cohort 2 students have co-funding. We are grateful for the support of:

- Compound Semiconductor Applications Catapult
- Compound Semiconductor Centre
- Huawei
- IQE
- Leonardo MW
- Linwave
- National Physical Laboratory
- Newport Wafer Fab Ltd.
- Qorvo
- The Rockley Group
- SPTS Technologies

We are actively seeking additional partnerships through conversations with companies about their research and development needs.

CDT students outside the Queens buildings at Cardiff University

EXPERTISE AT THE HUB

The CS Hub investigators and associated groups have been carefully selected for their track record in innovation and impact, complementary technical capability and the individual skill sets that can combine to create new solutions to the identified major scientific challenges in manufacturing. Expertise in epitaxial growth, including growth on non-native substrates is provided by Li, Liu, Missous, Wallis, and Wang. Buckle, Elgaid and Missous bring experience of wafer scale-up and manufacturing uniformity over these larger wafer sizes. Abadia, Beggs, Quaglia, Smowton and Tasker bring world leading expertise in design, integration and characterisation.

Leading Academics

In addition to the Hub's Work Package Leads, we work with a number of world-leading academics to develop the highest impact research possible under the remit of the Hub. Michael Pepper FRS, FREng (UCL) (h-index 55, 8 patents) is Pender Professor of Nanoelectronics and has received the Royal Society's Bakerian Prize Lectureship, Hughes and Royal Medals. He is co-founder and Scientific Director of THz technology spin-off company TeraView. He is a former member of General Board and Council of Cambridge University and Council for Industry and Higher Education.

Alwyn Seeds FREng, FIEEE (UCL) is Professor of Optoelectronics. He pioneered the research area of microwave photonics and was awarded the Gabor Medal and Prize of the Institute of Physics in 2012. He is an inventor on 16 patents and is co-founder of Zinwave Ltd, which is now the third largest supplier of wireless over fibre systems in the world and was acquired by McWane Technologies Inc. in 2014.

These staff are supported by academics Rick Smith & EPSRC Manufacturing Fellow Jon Willmott (Sheffield), Max Migliorato (Manchester), and Senior Research Fellows Siming Chen, Minchu Tang (UCL) and Sang Soon Oh (Cardiff) covering design, nitride fabrication, and characterisation and growth of CS on Si.

Flexibility

The Hub has worked flexibly to ensure that our research remains highly relevant in the constantly evolving CS manufacturing environment. We have welcomed several new people to the team, bringing with them a variety of expertise essential to keep the Hub at the very peak of research excellence. Dr Sara-Jayne Gillgrass has taken over leadership of Work Package 2 (Fabrication) from Dr Daryl Beggs. Sara-Jayne brings expertise in design, development and fabrication of lasers, VCSELs and other integrated photonic devices. Dr Craig Alford has taken over leadership of Work Package 3 (Fast Fabrication and Characterisation) from Dr Sam Shutts. Craig brings expertise in the development and automation of systems for the characterisation of electronic and optoelectronic devices. Sara-Jayne's and Craig's management of work packages are good examples of progression within the Hub.

Above: Sara-Jayne Gillgrass, WP2 lead.
Below: Craig Allford, WP3 lead

New expertise

The Cardiff lab team have also been joined by a new post-doctoral research associate, Dr Yun Long. Dr Yun bring expertise is in semiconductor optoelectronics, with a background in materials characterization. Hub associated PhD student, Wei Zhong, joined the Hub (Sheffield) this year, working on Direct Epitaxy to achieve ultra-high efficiency and ultra-high resolution microdisplay. Calum Dear (UCL) is working on MBE-grown 1550-nm III-V quantum-dot materials and devices on Si substrate for Si photonic systems. Makhayeni Mtunzi (UCL) will work on III-V quantum dot lasers grown on patterned silicon and SOI substrates by MBE.

Materials Growth (Epitaxy)

Summary: Work package 1 brings together all the compound semiconductor growth activities being undertaken with in the Future CS Manufacturing Hub. This covers a diverse range of materials systems, including Nitrides, Arsenides and Phosphides. A key focus of this work is growth of device structures on to substrates such as Silicon that are compatible with, low cost, large volume manufacturing to allow exploitation of the technologies in commercial markets.

Lead: Prof. David Wallis; Email: WallisD1@Cardiff.ac.uk
Contributing academics: Tao Wang (Sheffield), Mo Missous (Manchester), Huiyun Liu (UCL), and Qiang Li (Cardiff). We also have 2 project partners; Prof. Manus Haynes (Lancaster) and Dr Philip Shields (Bath), who are working on a Future CS Hub sponsored feasibility studies.

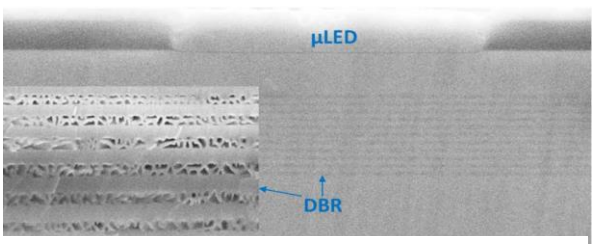
WP1 encompasses all the epitaxy activities that are relevant to the CS Hub. By bringing together the research activities at different universities, experience and best practice can be shared across the groups to solve problems and extend individual capabilities.

Progress and challenges: Last year saw all of the university growth Laboratories closed due to Covid restrictions in March 2020. As these restrictions have been lifted, limited occupancy rules have also had an impacted on the ongoing experimental research activities of the research teams. Whilst this has inevitably slowed down the Hub activities, some significant developments have been achieved: Several of the labs have taken the opportunity to upgrade their growth reactors with both Sheffield and Cardiff installing new in-situ measurements systems to enable real time monitoring of their growth processes. This will allow significant improvements in the control and understanding of how the epitaxial structures develop. In the last update we also highlighted that Professor Huiyun Liu at UCL had won funding for a new MBE system dedicated to the growth of Arsenide structures with low background impurities. The commissioning of this new system was completed, and will provide new opportunities to improve the performance of the quantum-dot laser structures being developed in Prof. Liu's group.

In the field of Nitrides, Prof. Tao Wang at Sheffield has developed a method to grow Distributed Bragg Reflection (DBR) structures for Nitride based Vertical Cavity Surface Emitting Lasers (VCSELs). Following growth, electro chemical etching is used to increase the reflectivity of the DBR by porosification of the layers. This can be combined with a novel regrowth technology developed for high performance micro-LEDs to give micro VICSELs which so far have shown very low optical lasing thresholds.

Image of the New MBE system commissioned at UCL

Work in Professor Mo Missous' group in Manchester is focused on the development of Metamorphic High Electron Mobility Transistor (HEMT) structures for magnetic sensing applications. Current materials work is looking at the development of highly strained (3.2%) InAs quantum well structures which promise to give higher carrier concentrations and mobilities which will further enhance the sensitivity of the magnetic sensors being developed.



Porous DBR structures for a Nitride based VCSEL

Scaling Fabrication & Photonic Devices

Summary: This work package is addressing the key challenge of fabricating high quality and reproduceable compound semiconductor devices over large format wafers. A particular focus is the fabrication of devices such as VCSELs and passive components on GaAs substrates to allow, low cost, large volume manufacturing of the devices being developed in other work packages in the Manufacturing Hub.

Lead : Dr Sara-Jayne Gillgrass Email: gillgrasss@cardiff.ac.uk
Contributing academics: P. Smowton, C. Allford, S. Shutts, P. Buckle, Q. Li, K. Elgaid, M. Missous.

In work package 2, we are dedicated to developing reliable and reproducible fabrication processes, particularly across large format wafers (>100 mm). We are also focussed on more complex fabrication involving multi-level processes and novel photonic integration. Working alongside colleagues at Cardiff University's Institute for Compound Semiconductors (ICS) allows for knowledge transfer and innovation and the use of cutting-edge fabrication facilities for wafer diameters (currently) up to 150 mm.

Progress and challenges: Passive capacitor, inductor and resistor components are necessary to realise GaN monolithic microwave integrated circuits (MMICs) of WP5 and the on-chip circuits integrated with the detector arrays of WP7. Fabrication of components where topography can hinder uniformity in standard photolithography processes can be challenging, accounting for previously seen high failure regions on the wafer during characterisation. A MicroWriter ML3 Pro from Durham Magneto Optics has recently been installed providing a maskless lithography technique that should reduce contamination and improve wafer scale uniformity where underlying topography is a problem. We will investigate the use of this tool for WP2.

We have established a 150 mm VCSEL fabrication process in collaboration with ICS, with repeatability and timeliness of the process demonstrated across multiple parallel wafers. An example of one of these VCSEL wafers is seen in figure 3 below. Automatic probing at the wafer level across these 150 mm wafers reduces cost and speeds up development of material and process characterisation. Results from 150 mm VCSEL wafers were disseminated at SPIE Photonics West 2021 [1].

An example of a photonic device included in this work package is shown in figure 1. Complex, multi-level processing is demonstrated with dielectrophoretic electrodes above and below a buried 3-D SU-8 channel, all integrated on a III-V active platform with on-chip light sources and photodetectors for sensing applications. Other photonic devices being developed include array structures based on III-V nanowires grown, by Dr Qiang Li, on SOI substrates, providing alternative solutions for light sources in integrated photonic circuits.

[1] D. Hayes et al., Proc. SPIE 11704, Vertical-Cavity Surface-Emitting Lasers XXV, 1170406

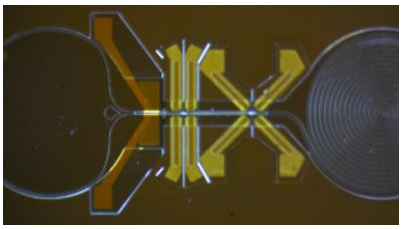
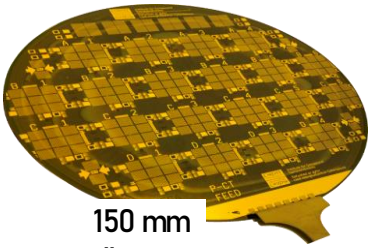


Figure 1. Integrated active III-V photonic platform with dielectrophoretic elements and 3-D buried channel for sensing applications.



150 mm diameter

Figure 3. One of the batch processed VCSEL wafers.

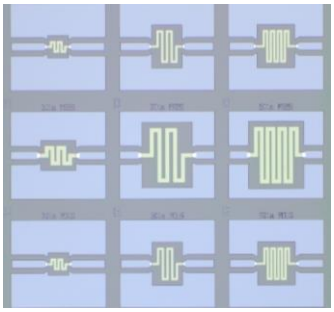


Figure 2. Initial development of passive components using the direct laser writer after NiCr lift-off and exposed resist for feed metal patterning.

Fast Fab and Characterisation

Summary: Recent technical and scientific challenges have involved: fast-fab of vertical cavity surface emitting lasers (VCSELs); scaling up characterisation for optical devices using auto-probe wafer-mapping; reporting degradation mechanisms of III-V lasers on Si, testing and expanding existing device degradation studies; characterising the behaviour of 1550nm InAs QDash lasers grown directly on (001) silicon substrates and developing fabrication and measurement techniques for mode-locked lasers.

Lead: Dr Craig Allford; Email: AllfordCP1@Cardiff.ac.uk
Contributing academics: N. Abadia, K. Elgaid, H. Liu, M. Missous, R. Quaglia, S. Shutts, R. Smith, P.M. Smowton.

The aim is to develop fast fabrication and characterisation techniques to feedback to design and growth, minimising development cycle time. The key work package deliverables include, reliability measurements (III-Vs on Silicon), fast-fab on large area VCSEL wafers, in-line characterisation to support integration.

Progress and challenges: The previously established 200mm wafer-scale semi-automated auto-prober measurement system has been further developed to provide a rapid characterisation capability for compound semiconductor optoelectronic devices, thus reducing costs and increasing the speed of material and process characterisation. This system has been used to measure several 150mm fully fabricated VCSEL wafers in a collaboration between wafer supplier IQE Plc, fabrication facility Cardiff University's Institute for Compound Semiconductors (ICS) and CS Hub WP2 & WP3. The measurements provide invaluable feedback on the quality and uniformity of the manufacturing process for fully fabricated VCSEL devices.

We have also further developed a fast turnaround VCSEL fabrication and characterisation process, which uses a reduced number of fabrication steps and can provide valuable data on epitaxial growth quality and uniformity on a timescale that is advantageous for manufacturers, thus further improving wafer yield and reducing costs. A series of fast turnaround VCSEL devices have been measured via wafer-scale mapping, and a selection of further advanced characterisation. The results have been directly compared to fully fabricated VCSEL devices and this work was presented at the international SPIE Photonics West 2021 conference (Proc. SPIE 11704, Vertical-Cavity

In collaboration with colleagues at the Hong Kong University of Science and Technology (HKUST), CS Hub researchers have fabricated and characterised indium arsenide (InAs) quantum dash lasers grown on silicon substrates, operating at 1550 nm. The published results (Appl. Phys. Lett. 118, 131101 (2021)) show that whilst there is room for improvement in laser performance in this early research stage, the intrinsic performance of the material is better than more mature InAs quantum dot lasers grown on gallium arsenide which operate at 1300 nm. Therefore there is excellent promise to further develop optoelectronic devices based on this material system to exploit the potential for larger wafer sizes and improved integration a silicon based platform will offer for applications in e.g. telecommunications.

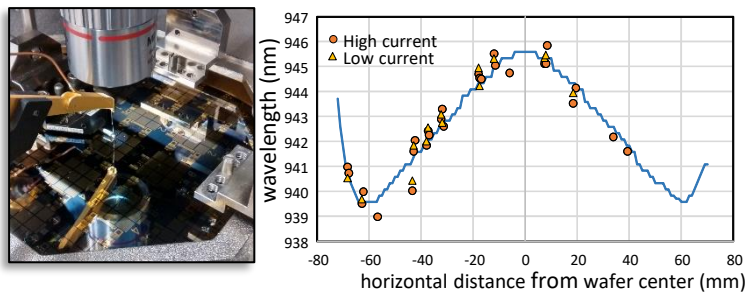


Figure 1: (above) The 200mm auto-prober characterising a 150mm VCSEL wafer developed and fabricated via ICS and WP2.
(above right) The measured peak emission wavelength of VCSEL devices against the Fabry-Perot dip in measured reflectance data across a 150mm wafer.

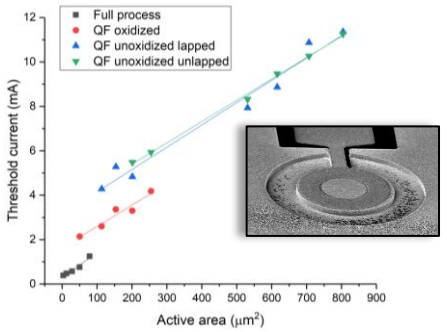


Figure 2: A comparison of the measured threshold current against device active area for full process and quick-fab (QF) VCSEL devices. A scanning electron microscope image (SEM) of a QF device is also shown (inset).

Manufacturing Technology for Optical Data Communications on Silicon

Summary: Continuous development has been on-going pursuing the high performance of silicon-based InAs/GaAs quantum dot (QD) lasers in this work package. Here, we reported recent progress of the growth of InAs/GaAs QD lasers on CMOS compatible on-axis Si (001) substrates, and the demonstration of high lasing operation up to 130 °C, which is the upper limit of our temperature controller.

Lead: Prof. Huiyun Liu; Email: huiyun.liu@ucl.ac.uk
Contributing academics: Prof. Peter Smowton, Prof. Alwyn Seeds, Dr Qiang Li, Dr Siming Chen, Dr Sam Shutts

In work package 4, we are dedicated to develop high performance InAs/GaAs QD lasers monolithically grown on Si substrates with optimised gain per unit length (for high frequency), increased operation temperature (>125 °C) and low current CW operation at 20 mW optical output power. This has been approached via multiple growth techniques, such as exploiting p-type modulation doping, optimizing/combining nucleation layer, dislocation filter layer as well as thermal annealing, which shows promising initial results. In the period of last 12 months, we further developed growth techniques, which aims at minimizing the impact of the two critical defects existed in III-V/Si, namely antiphase boundary (APD) and cracks. Furthermore, a new III-V MBE system has been commissioned for high-performance III-V/Si devices in this work package.

Progress and challenges: The APD-free III-V growth on on-axis silicon (100) substrate renders III-V photonic materials and devices compatible with the mature CMOS technology. By using the twin MBE system, we have developed III-V buffer growth on on-axis silicon (100) substrates. It is found that a Si epilayer is critical for the effective annihilation of antiphase boundaries for GaAs growth on silicon substrates, and the mechanism behind it is explained for first time [Adv. Optical Mater. 8, 2000970 (2020)]. The Figure 1 shows the annihilation of APDs at different GaAs buffer thickness on the samples with and without Si buffer. These proof-of-concept results enable a promising route of low-cost and high-density Si-based photonic integrated circuits.

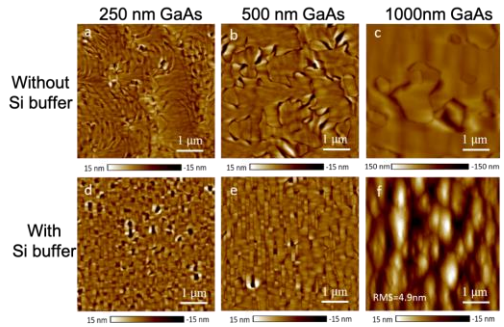


Figure 1. 5μm×5μm AFM images of GaAs with different thickness monolithically grown on deoxidized Si substrate with and without Si buffer layer.

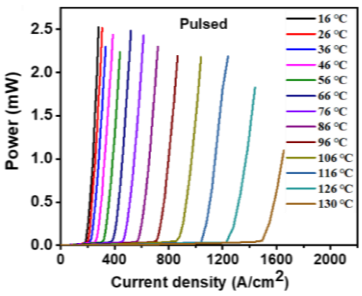


Figure 2. Light-current measurements of laser at various temperatures under pulsed mode.

Building on the III-V-on-Si growth technology, we further developed a growth scheme to handle the crack issue. It was done via implementing the InAs/GaAs QD growth on Ge/Si virtual substrates with 300nm Ge buffer. The threading dislocations generated at the Ge/Si interface have a significant lower density in the thin Ge layer as a result of high temperature cyclic thermal annealing. This effectively reduces the total thickness of the III-V layer while maintaining a low TD density level, and hence could significantly enhance the yield of laser devices while not degrading their performance. As shown in Figure 2, lasing up to 130 °C was achieved for the InAs/GaAs QD laser grown on Ge/Si virtual substrate. To the best of our knowledge, this lasing operation temperature (130 °C) is the highest operating temperature for lasers monolithically grown on silicon.

A new MBE system dedicated to the growth of InAs/GaAs QD laser structures has been installed in UCL. This will accelerate the process of technical development and wafer deliverables for this work package.

Advanced Radio Frequency Devices & MMICs

Summary: Building on on-going success, the aim of this work package is to demonstrate a UK GaN-on-Si GaN based HFET technology baseline. Specifically targeting wireless applications, this work package aims to ultimately establish a full GaN-on-Si HFET device, a collection of passive devices and a MMIC technology platform suitable for high to medium power microwave 5G system applications. This work package uses high-frequency device characterisation at staged points to allow feedback for the optimisation of the epitaxial growth to deliver device performance and a fully integrated on-chip technology in line with industrial requirements. Work package activities are closely aligned with major compound semiconductor manufacturing industry partners including Newport Wafer Fab (NWF), IQE, SPTS and the CSA Catapult.

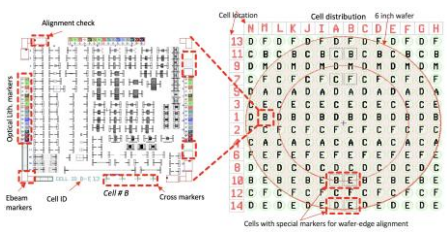
Lead: Prof. Khaled Elgaid
Email: ElgaidK@Cardiff.ac.uk
Contributing academics: Prof. Paul Tasker, Dr. Johnathan Lees & Dr. Roberto Quaglia

The WP5 focus is to develop advanced GaN on Si RF active and passive devices and implement them through the realisation of high-performance MMICs for wireless high data rate communications systems. The technology development in this WP is aimed at addressing industry requirements and utilising full wafer process methods. Strong links have been formed with several key industry partners in both areas of technology, such as process monitoring and verification, as well as design, where component specifications requirements are defined. Key industry interactions include Newport Wafer Fab, SPTS, IQE, MBDA, CSA Catapult, Leonardo and IconicRF.

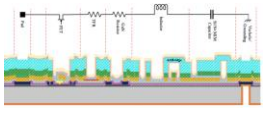
Progress and challenges: An alternative solution to RF GaN on SiC is to use GaN on Si substrates, hence large (>300mm), lower-cost and the potential of volume production. These advantages of GaN on Si come at the cost of lower performance in comparison to GaN on SiC, due mainly to losses in the substrate (challenges in the realisation of low-loss MMIC interconnect and passive structures), large lattice mismatch (larger wafer-bow and challenges in fabrication) and relatively poor thermal conductivity. Irrespective of the substrate used, to obtain high intrinsic performance RF GaN devices, there is the need to develop a short-offset gate lengths of ≤ 0.25um aligned in a source/drain gap of ≤ 5µm technology. Ensuring a corresponding increase in extrinsic performance requires RF parasitics to be minimised, optimisation of the epitaxial layer, layout optimisation, minimisation of ohmic contacts /access resistances and development a robust PDK. Advanced RF devices & MMIC technology realisation has so far been progressed in two stages; firstly by developing the necessary fabrication modules for active and passive devices on partial wafers, and then device characterisation and evaluated on different epitaxial layer structures. Now a full 6 inch wafer process now has commenced.

To address the key RF GaN technology development challenges, the research team have carried out essential development; reliable photo lithography for small features/gaps, an aligned gate in ≤ 5µm HEMT, reducing access resistance while maintaining power performance, ohmic contacts development using source/drain recess - published *"Optimization of ohmic contact for AlGaN/GaN HEMT on low-resistivity silicon", 2020, IEEE TED, fabricated and characterised devices on partial wafers.* Working with multiple industry partners and linking with other projects developing RF GaN on SiC (the GaN*for*CS project), a process development kit (PDK) is being developed to allow the simulation and design of active circuits,). **Figure 1** shows a top-view of full 6-inch layout mask-set to allow for a robust PDK development. The aim of next stage of development will be based around wafer-level and PDK realisations with more involvement by industry partners.

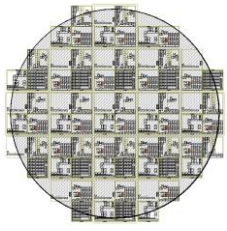
Figure 1 shows a top view of full 6-inch layout & technology



#	Devices	# of cells
A	Capacitors FETs	13
B	Capacitors FETs	16
C	Actives PCMs	34
D	Inductors	27
E	MS lines	18
F	Resistors	25



Planned MMIC Technology



Complete mask design layout for 6'' wafers

Monolithic Integration of Micro-emitters and HEMTs for Microdisplay and Li-Fi

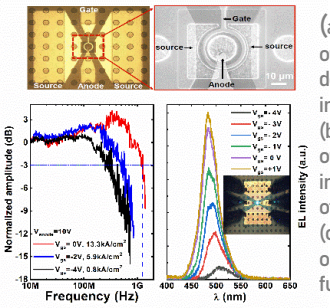
Summary: Building on the work in the platform our approach is to develop a direct epitaxial technique to integrate III-nitride micro light emitting diodes (μLEDs) and HEMTs on a single wafer in order to demonstrate and then manufacture monolithic on-chip integration of μ-LEDs and HEMTs for ultra-high resolution & ultra-high efficiency micro-displays and ultra-fast & zero cross-talk Li-Fi; We will continuously develop industrial compatible epitaxial overgrowth steps to integrate CS/Si structures with different designs on the same substrate.

Lead: Prof. Tao Wang; Email: t.wang@Sheffield.ac.uk
Contributing academics: Prof. Huiyun Liu, Prof. Alwyn Seeds, Dr. Rick Smith, Prof. Peter Smowton, Prof. Khaled Elgaid

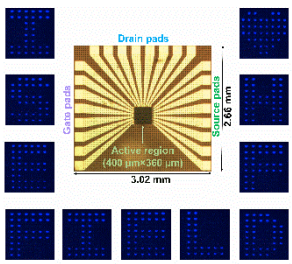
LiFi exhibits striking advantages compared with current WiFi technology in terms of bandwidth, data transmission speed. The major component of LiFi is visible LEDs which need to have ultra-fast response time and need to be controlled by high frequency electronic components. The most promising approach to achieving high bandwidth and high data transmission rate for LiFi to utilise μ-LEDs. Furthermore, AR & VR microdisplays, smart watches and smart phones require μLEDs with an ultra-small dimension, high EQE and narrow spectral linewidth. An on-chip epitaxial Integration of III-nitrides μLEDs and HEMTs on low cost and up-scalable silicon substrates for LiFi and microdisplays is the best way forward, where each μ-LED transmitters can be individually controlled by GaN based HEMTs uniquely.

Progress and challenges: In order to achieve high modulation bandwidth and high data transmission rate, μLEDs need to be driven at a high injection current density on a kA/cm^2 scale, which is ~3 orders of magnitude higher than those for normal visible LED operation. μLEDs which are traditionally fabricated by dry-etching techniques suffer from dry-etching induced damages, leading to both a substantial reduction in performance and great challenges to viability at a high injection current density. Conventional biasing generates a great challenge for a single μLED, which needs to be modulated at a high injection current density and at a high frequency. Due to the similar reasons, a heterogeneous integration approach for the fabrication of microdisplay (such as Pick-and-Place and a combination of μLED and CMOS) is far from requirements.
We aim to develop a direct epitaxial technology to manufacture a monolithic on-chip integration of μLEDs and HEMTs for microdisplays with ultra-high resolution & ultra-high efficiency (> 20% EQE, ≤ 5 μm pixel and ≤ 2 μminter-pitch) and a LiFi system with ultra-fast (>2 GHz) and zero cross-talk. We also aim to establish and then develop a spinout into a global manufacturer of monolithic on-chip integration systems.

Achievements:
(1) Demo the 1st direct epitaxy approach to achieve ultra-small and ultra-compact μLED arrays with a record EQE and the narrowest spectral linewidth (3.6 μm in diameter, 2 μm in inter-pitch and 9.5 % Max. EQE); [1]
(2) Demo a direct epitaxy approach to achieve the 1st monolithic on-chip integration of a single μLED and a HEMT with a record modulation bandwidth of 1.2 GHz;[2]
(3) Demo a direct epitaxy approach to achieve the 1st monolithically integrated 8 × 8 μLEDs & HEMTs microdisplay; [3]



(a) Optical microscope image of our monolithically integrated device with a zoom-in SEM image;
(b) 3dB modulation bandwidth of our monolithic on-chip integrated device as a function of gate bias under V_{anode} = 10 V;
(c) EL spectra of our monolithic on-chip integrated device as a function of gate bias.



(a) Optical microscopic image of our 8 × 8 integrated μLEDs & HEMTs microdisplay
(b) Images ("I ♥ Sheffield") which are captured from the short video our 8 × 8 integrated μLEDs & HEMTs microdisplay.

light emitting diodes (μLEDs) with a narrow spectral linewidth", ACS Nano 14, 6906 (2020);
2. "Direct epitaxial approach to achieve a monolithic on-chip integration of a HEMT and a single μLED with a high modulation bandwidth", ACS Appl. Electron. Mater. 3, 445 (2021)
3. "Monolithically integrated μLEDs/HEMTs microdisplay on a single chip by a direct epitaxial approach" Adv. Mater. Technol. DOI: 10.1002/admt.202100214 (2021);

Magnetic Arrays

Summary: The approach is the integration of high electron mobility, high magnetic sensitivity 2DEG structures with on board analogue and digital electronics to deliver scanning magnetic imaging systems for Non-Destructive Testing of metallic and composite materials

Lead: Prof M.Missous; Email: m.missous@manchester.ac.uk
Contributing academics: Dr M. Migliorato and Dr P. Buckle

The overarching theme of WP7 is magnetic imaging of ferrous and non-ferrous materials and lately composites. The work follows a vertically integrated approach starting from epitaxial growth of advanced 2DEG structures with tailored magnetic sensitivities to device fabrication of integrated arrays and passives, packaging and finally system integration for imaging of flaws, defects and microstructures (See Figure 1 below).

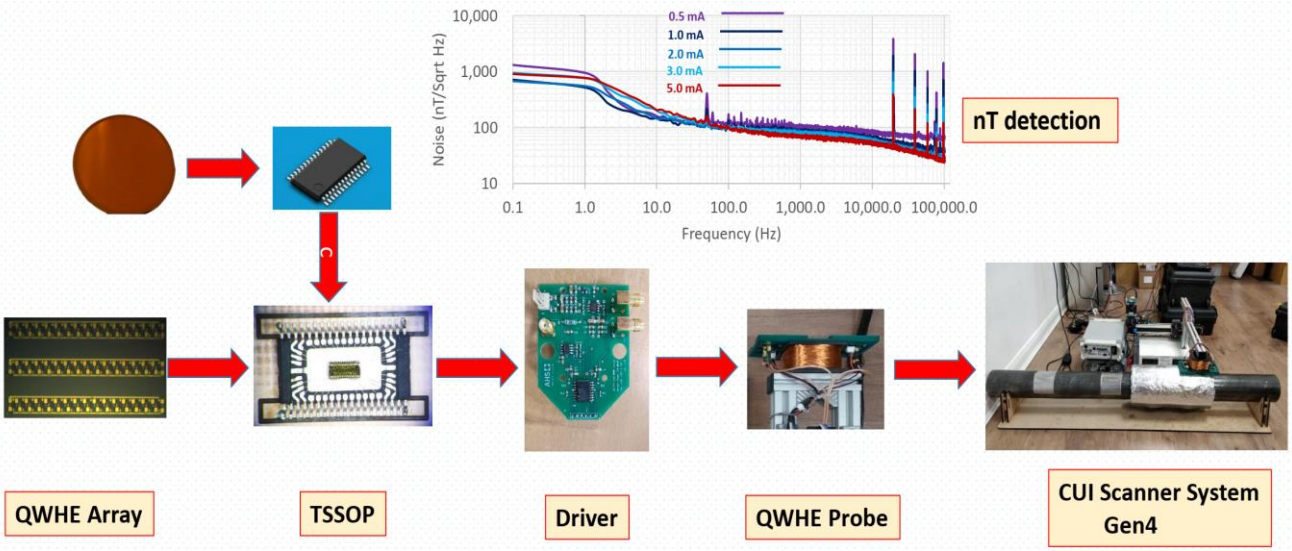


Figure 1 Vertical integration of magnetic imaging of corrosion under insulation

Progress and challenges: During the period magnetic imaging modality using Quantum Well Hall Effect sensors (QWHE) for were extended to study composites. The work to date has led to ~ 14 journal publications and over 30 conference presentations spanning from epitaxial growth to full system demonstrations with key challenges being imaging and classifications of flaws and defects in metals and composites.

Impact has been very strong as demonstrated in 6, separate, fully funded collaborative INNOVATEUK projects with [Renishaw, TWI, EtherNDT, FarUk, Wright, Home office, BAESystems] in imaging corrosion under insulation in steel and flaws and fibers in composites. as shown in Figure 2 below

The work to date in WP7 has now extended from ferromagnetic (and non-ferromagnetic) to composite materials to detects flaws and microstructures spanning the frequency range 50Hz to 2MHz.

The work on composite materials uses conductivity as the imaging modality which has necessitated the use of very high frequency (MHz) interrogation techniques. The high frequency techniques also result in much more compact imaging systems that are ideal for aerospace applications.

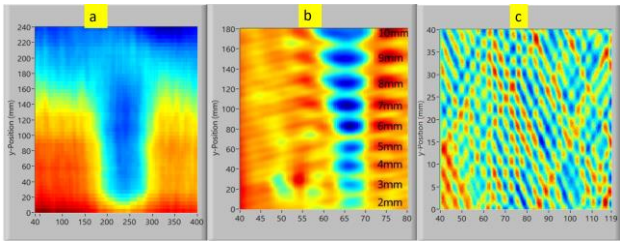


Figure 2 metallic imaging of (a) corrosion under insulation and (b) flaws in composites and (c) fibres in composites

Generic Photonic Integration

Summary: Work Package 9 comprises of generic photonic integration work on proof-of-concept optoelectronic devices and systems. The short-term driver for this technology is the provision of GaAs-based integrated optoelectronic devices and systems for interconnects used in aerospace and nuclear sectors and ultimately for telecommunication networks in the long-term.

Lead: Dr Nicolás Abadía; Email : abadian@cardiff.ac.uk
Contributing academics : Prof. Huiyun Liu, Prof. Dame Xiang Jane Jiang, Dr Haydn Martin, Prof. Tao Wang.

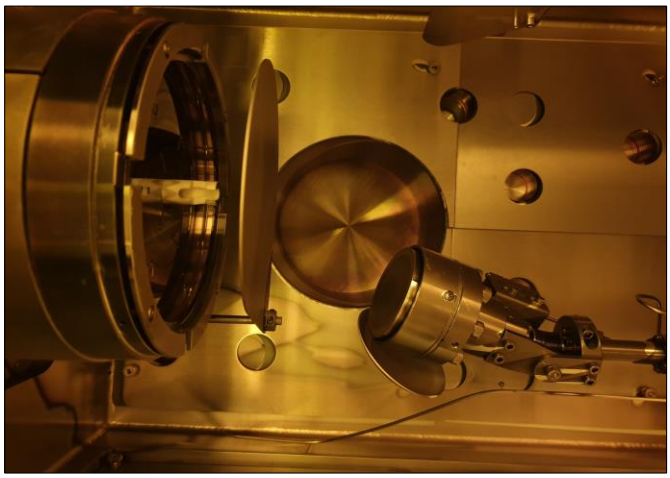
Generic Photonic Integration is a platform that allows the production of photonic integrated circuits (PIC). PICs are similar to the electronic integrated circuits used in computers and other electronic devices. The main difference between the photonic integrated circuit and the electronic integrated circuit is that the former works with light and the latter works with electricity.

The invention of the integrated electronic circuit was in the United States in 1958 and revolutionised electronics and our daily lives. The field progressed very quickly from very basic old computers used in big research facilities to a wide range of systems used in our daily life: mobile phones, tablets, laptops, WiFi and the Internet, etc. In a similar way, PICs will revolutionise several fields including next generation telecommunication networks like the Internet or the mobile network.

PICs can drastically increase the capacity and reduce the cost and power consumption of networks. This will allow the streaming of 4K content to your computer and smart TV or the development of the next generation mobile network (know as 5G), which will allow the implementation of new services like the self-driving car, telesurgery or portable virtual reality.

Progress and challenges

- New collaboration with the EPSRC Future Metrology Hub including the University of Huddersfield
- Reinforced links with University College London and the University of Sheffield
- Several invited seminars, visits and workshops
- There has been progress on the design of the modulator
- Several devices will be radiated. The progress has been affected by Covid.
- There has been progress on the fabrication of the GaAs waveguides.



Loading of the chamber of the Lesker Pro-Line PVD200 to development of the ITO process.

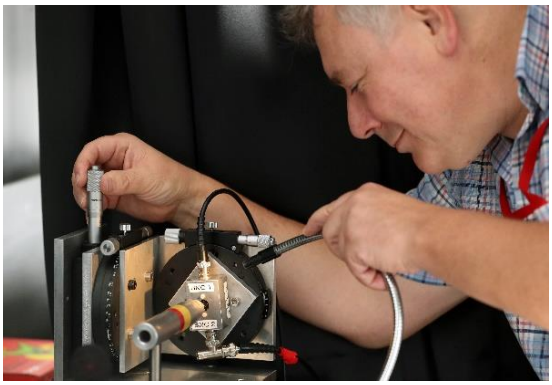
Rounds 1, 2 and 3

During the Hub's second year, we released our first call for applications to our feasibility study fund. This fund, totalling £1M (full economic cost) was reserved for new studies which push the boundaries and contribute to the strategy of the Hub. The aim of funding these feasibility studies is to broaden the reach of the Hub by encouraging new academic and industry partnerships, whilst supporting new cutting-edge research which is complementarity to and aligns with Hub objectives.

We originally envisaged supporting up to 10 projects of average length of 7.5 months; however we have used the flexibility available to us to set out a more extensive strategy for engaging with new partners and delivering key performance indicators via feasibility study funding.

Funding plan

Round 1, the studies funded during which have concluded, called for applications of up to £40k (80% full economic cost) over 6 months. This was followed with an opportunity for successful round 1 studies to apply for up to £96k (80% full economic cost), with this funding intended to lead to and facilitate a large scale EPSRC or Innovate UK grant application with strategic alignment to the Hub. These studies would build on successful feasibility studies and deliver additional key performance indicators for the Hub.



This was followed by a third funding round, coordinated with funding calls from other future manufacturing Hubs in order to encourage the possibility for collaborations involving multiple Hubs. This provided an opportunity to apply for up to 50k (80% full economic cost). This final call invited new applications from areas that overlap between the Hubs, strengthening the links amongst them and promoting interaction, as well as delivering value for money.

Evaluation of applications for funding

The Hub Management Board (MB) hold responsibility for awarding funding for feasibility studies and have taken the advice of the Hub's Strategic Advisory Board in assigning funding to applicants. Applications for the first round of funding were prioritised for funding according to the delivery of new academic and industrial collaborators, and were then scored on:

- Scientific Quality and Clarity
- Potential Impact/Opportunity
- Hub Alignment

These criteria were used to enable new academic collaborators to request funding for new and innovative research projects which were aligned to the Hub strategy.

Funded applications

Six studies were awarded round 1 feasibility study funding. They began their journey with the Hub in August 2018 and were 6 months in duration. The Hub invested £229,992 in the novel studies and details of each feasibility study can be found in the Hub's 2019 annual report: https://compoundsemiconductorhub.org/downloads

In the second round, to enable the most promising of these studies to continue their work with the Hub, 4 continuation studies were awarded funding and their studies commenced between August and October 2019, with durations between 12 and 18 months. The Hub invested £376,806 in the continuation studies and details of each continuation study can be found in the Hub's 2020 annual report: https://compoundsemiconductorhub.org/downloads

In the final round, the Hub invested a further £247,799 in 5 new studies as part of a joint feasibility call with other future manufacturing Hubs. These projects started from April 2020 onwards, with a duration of 6 months although all projects have incurred delays due to Covid. The studies are listed below and descriptions can be found on the pages that follow this.

£229,992 Invested in initial 6 feasibility studies

£376,806 Invested in 4 continuation studies

£247,799 Invested in 5 new feasibility studies

£854,597 Total investment

2020 Hub-funded feasibility studies

PI	Insitiutions	Title
Dr Philip Shields	University of Bath	Manufacturing of large-area InP on nano-V-grooved CMOS-compatible Si
Dr Kean Boon Lee	University of Sheffield	Novel GaN-based Vertical Transistors for LED Driver Applications
Dr Nicolás Abadía	Cardiff University	Measurement of Carrier-Induced Electro-refraction in InAs/In(Ga)As Quantum Dots
Dr Antonio Hurtado	University of Strathclyde	Vertical-cavity LASER arrays for BRAIN-inspired photonics (LASERBRAIN)
Dr Vishal Ajit Shah	University of Warwick	Semi-insulating SiC epitaxy on SiC and Si substrates, for monolithic integration of GaN "on insulator" RF technology and high voltage SiC devices.

The 2020 feasibility study: Measurement of Electro-refraction in Quantum Dots study, led by Dr. Nicolás Abadía has been delayed due to Covid and facilities not being able to grow wafers. The project aims to verify strong electro-refraction in quantum dots experimentally. This research will enable more efficient phase shifters to improve Mach-Zehnder Interferometers, and there will be more information on the project's research in next year's annual report.

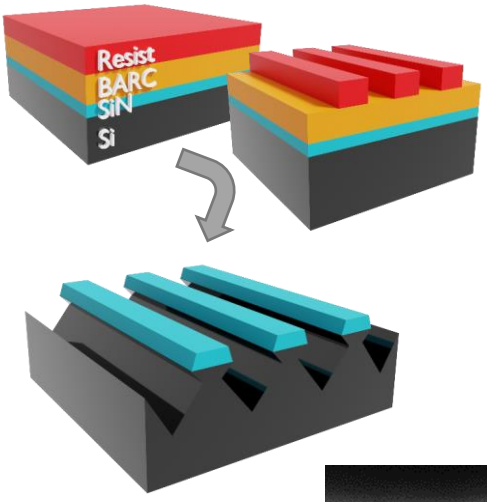
Manufacturing of large-area InP on nano-V-grooved CMOS-compatible Si

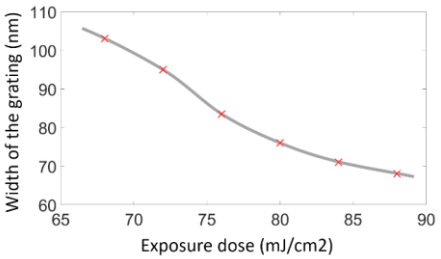
Lead applicant: Dr Philip Shields, University of Bath
Co applicant: Dr Qiang Li, Cardiff University

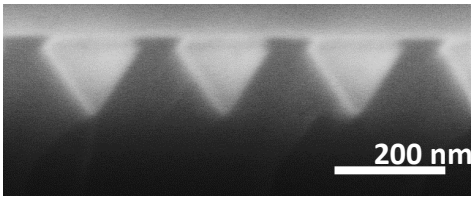
Summary: This project aimed to demonstrate the feasibility of the metamorphic growth of InP on nano-V-grooved CMOS-compatible Si (001) substrates. The integration of (001) silicon and direct band-gap III V semiconductors is critical to provide a viable material platform for photonic integrated circuits and to allow the scale-up to the larger diameters offered by silicon substrates and subsequent cost reduction. We aimed to exploit the large-area nanolithography technique of Displacement Talbot lithography to pattern linear grating structures on silicon substrates with feature-sizes down to 100 nm with a 250 nm pitch, and demonstrate this at the wafer scale. We would then use these features to create V-grooves that would offer the opportunity, following the subsequent growth of InP materials by metal-organic-chemical vapor deposition (MOCVD), to remove antiphase-boundaries, confine interfacial defects and achieve device-quality thin films.

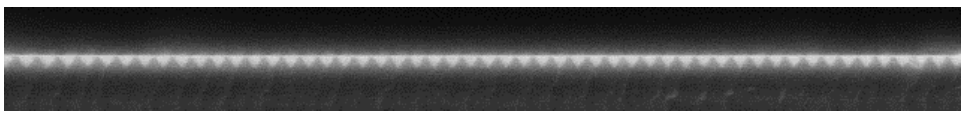
Outcomes/major findings: n this project we developed a lithography process that would allow the patterning of a 250 nm pitch grating across a full 100 mm wafer. The process parameters were explored to allow us to control the grating dimensions in the range from c. 70-100 nm by carefully controlling the exposure dose. Plasma etching was then used to transfer the pattern through an anti-reflection coating, required for reliable patterning, into a thin silicon nitride layer that would serve as a mask during the wet-etching of the silicon substrate. Very careful attention was required to control the plasma over-etching into the silicon in order to finely tune the wet etching process. The V-grooves in silicon were achieved by using a selective facet-dependent etch chemistry. Process challenges included optimising the resist thickness to avoid resist collapse, controlling the evolution of the critical dimensions, dealing with unwanted side-effects of plasma etching, and stripping mask materials sufficiently without prejudicing subsequent processes. Further work is required to generate sufficient material for growth optimisation.

Relevance to manufacturing: Demonstrating small regions of V-grooves, even accidentally, is much simpler than developing a reproducible process for manufacturing that is uniform at the wafer scale. For the sub 100 nm feature sizes required in this project, the inherent non-uniformity of each sequential process step could be compounded towards an unacceptable final result. To counter this, uniformity must be assessed at each step and the full process designed to rely on self-homogenising steps such as etch stop layers and self-limiting processes.









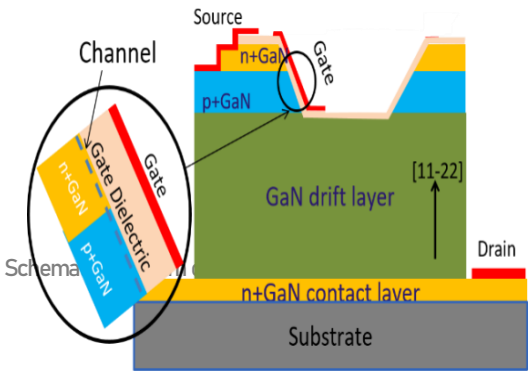
(Top left) Process schematic showing initial layer stack, lithography process and wet-etching steps. (Top right) Exposure control of the grating linewidth. (Bottom) SEM images showing fabricated V-grooves and their longer-range uniformity

Novel GaN-based Vertical Transistors for LED Driver Applications

Lead applicant: Dr Kean Boon Lee, University of Sheffield
Partners: Plessey Semiconductors Ltd
Hub Mentor: Prof. Tao Wang

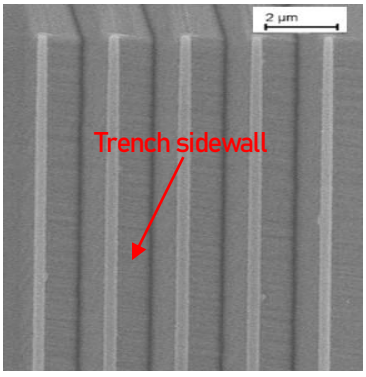
Summary: Next generation solid-state lighting will demand both high efficiency optoelectronics (LEDs) and highly compact and efficient driver electronics. Most of the driver electronics such as AC-direct LED drivers currently use Si-based devices for power conversions. These suffer from high on-state resistance/gate capacitances and hence high power losses and are not able to integrate monolithically with the optoelectronics.
This project aims to develop novel highly efficient vertical trench transistors which is compatible with integrated solid-state lighting on a semi-polar/non-polar GaN platform. The new fabrication technique enables low-index plane trench sidewalls using a self-stop wet etch method which greatly improves device manufacturability.

Outcomes/major findings: Traditionally, manufacturing the GaN-based trench vertical transistor requires a dry plasma etching technique which is expensive. The plasma etching process not only induces damage to the channel (active region) of the transistors which degrades the device electrical performance, it also lacks the etch selectivity and controllability which resulting in the device uniformity issues. To overcome these issues, we have developed a low cost manufacturing approach to fabricate semi-polar GaN trench vertical transistors using a hydroxide-based wet chemical etching technique. The trench sidewall plane orientation can be selectively revealed by aligning the trench to a particular angle during the etching process. A smooth c-plane sidewall has been achieved by aligning the

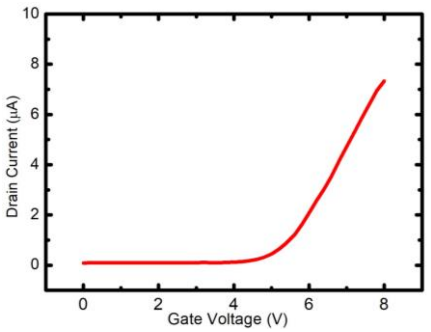


trench sidewall to the [1-100] direction. Formation of smooth sidewall is crucial for high channel conductivity in the transistors. Once formed, the sidewalls remain stable even after a prolonged etch. The 'self-stop' nature of the etching is important to ensure reproducibility in manufacturing. Employing this wet etch technique, we have successfully fabricated GaN-based vertical trench transistors and demonstrated the transistor actions with an enhancement mode operation. We are working with Centre for GaN Materials and Devices, University of Sheffield (future compound semiconductor manufacturing hub academic partner) to develop the semi-polar/non-polar GaN epitaxy structures for the vertical transistors.

Relevance to manufacturing: The novel fabrication technique greatly reduces the vertical transistor manufacturing cost and complexity without the need of the expensive dry plasma etching tools. This technique is compatible with the GaN LEDs fabrication processes, allowing monolithically integration of optoelectronics and electronic devices in the epitaxy and device levels for a highly compact solid-state lighting system.



SEM image of formation of trenches using the wet-etch technique for GaN vertical transistors.



Gate transfer characteristics of the fabricated vertical GaN trench transistor with a positive threshold voltage of +5V.

Vertical-cavity laser arrays for brain-inspired photonics (LaserBrain)

Lead applicant: Dr Antonio Hurtado, University of Strathclyde
Partners: IQE plc.
Hub Mentor: Prof Peter Smowton

Summary: The emulation of the human brain is the focus of profuse research effort for new computing paradigms. Whilst electronic techniques for neuronal models have been traditionally used, photonic approaches have recently emerged providing key advantages, (e.g. high bandwidths, low cross-talk); hence offering the potential to revolutionise neuromorphic (brain-like) computing. Notably, Vertical Cavity Surface Emitting Lasers (VCSELs) can display neuronal responses (e.g. spiking) but up to 1 billion times faster than neurons. VCSELs are low-energy and high speed devices permitting also their integration in compact 2D arrays; thus making them ideal for photonic neuronal models. In this project we focus on developing and investigating VCSEL-arrays with high emission wavelength uniformity. These will allow the future manufacturing of chip-scale neuromorphic networks of coupled laser neurons for key processing tasks (e.g. pattern recognition, image processing) whilst benefitting from ultrafast operation and low energy footprint.

Outcomes: The focus of the Feasibility Study (FS) is to (i) investigate 2-D VCSEL arrays with uniform wavelength emission and to (ii) describe new routes for neuromorphic photonic chips based upon uniform VCSEL arrays for brain-inspired computing.
During the FS project Hub partners at Cardiff Univ. developed different samples of VCSEL-Arrays comprised of up to 100 devices (10x10 arrays) operating at the wavelength of 940 nm. Optoelectronic characterisation setups were developed at Strathclyde for the analysis of the lasing threshold, optical power, spectral characteristics and light polarisation properties of the VCSELs in the array. Emphasis was given to the investigation of the emission wavelength uniformity of the VCSELs in the arrays. This is a key aspect for the future fabrication of network-scaled architectures of coupled VCSEL photonic neurons (emulating biological neuronal networks) processing information in a similar way as the brain does.
The left plot in fig. 1(a) shows the setup used for the analysis of the VCSEL-arrays. The insets at the right hand side in fig. 1(a) provide magnified images of a VCSEL-array (top) including the metallic contacts used to drive the individual VCSELs and a lens-ended optical fibre used to collect their emitted light (bottom). Fig. 1(b) plots the wavelength emission properties of a range of devices in one of the VCSEL-arrays investigated during the FS project.

Relevance to manufacturing; This FS project opens new research towards the fabrication and characterisation of novel chip-scale photonic systems with key-enabling VCSELs at their core for radically new neuromorphic computing and AI platforms. Such systems will permit adding 'intelligence' to photonic platforms; hence offering promise for transformative light-enabled hardware systems allowing the ultrafast processing of vast amounts of data. The knowledge derived from this FS project study will permit to describe practical routes towards the fabrication of key-enabling VCSEL-arrays with high wavelength uniformity for network-scale, coupled-laser systems for neuromorphic photonic computing functionalities benefitting from reduced footprint, low energy requirements for operation and ultrafast speed. Data obtained from the FS project has been used to support a successful application for an UKRI Turing AI Acceleration Fellowship.

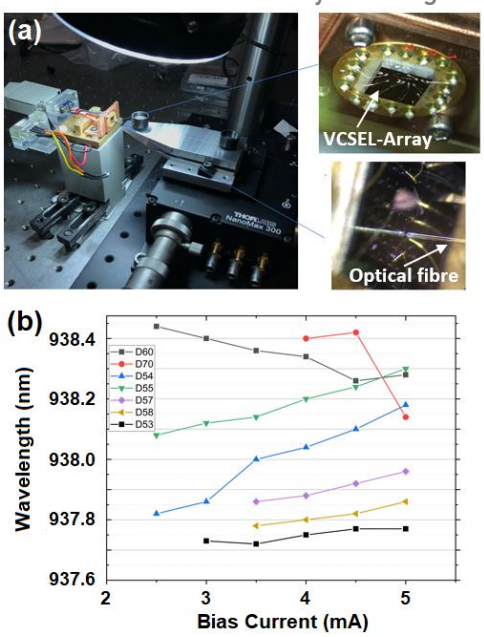


Fig. 1(b) revealed high wavelength uniformity for all individual VCSELs within the array (with levels well below a 1 nm wavelength span). Yet, for some functionalities higher uniformity approaching 0.1 nm or lower is desirable. Therefore, the preliminary results obtained during this FS project will be instrumental to enable a new range of highly wavelength uniform VCSEL-arrays, incorporating wavelength tuneability elements for full spectral control of the light emission of all integrated VCSELs.

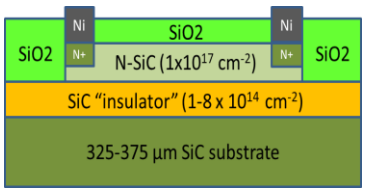
Feasibility of Semi-insulating SiC epitaxy on SiC and Si substrates, for monolithic integration of GaN "on insulator" RF technology and high voltage SiC devices.

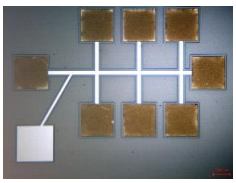
Lead applicant: Dr V A Shah, Warwick University.
Partners: University of Warwick, LPE Spa, CS Catapult, Agri Induction Ltd.
Hub Mentor: Prof. David Wallis

Summary: Silicon Carbide (SiC) and Gallium Nitride (GaN) are examples of Wide Bandgap (WBG) semiconductor materials which have recently entered the power electronics market, with the SiC power device market predicted to be worth $2bn by 2024. This growth is partially being driven by adoption of WBG devices in electric vehicles, where a high profile case study in the automotive sector is Tesla, who have adopted SiC MOSFETs and Schottky diodes in their DC-AC inverter. The clear strengths of GaN in the power market lies in the medium voltage range (300-900V) and for high frequency (>3GHz) applications, where the opposite is true for SiC (>1.2kV, <500kHz). If a platform could incorporate both materials, then hybrid device could be realised, utilising both strengths simultaneously in applications such as high power wireless charging.

In this project we are working towards the manufacturability of an innovative SiC/GaN on-insulator platform, which is completely compatible with standard manufacturing lines.

Outcomes/major findings: We have implemented two methods for achieving these "on insulator" platforms: i) materials growth using epitaxy through new gas sources, ii) selective implantation of various species. Both of these techniques have been implemented on 4H-SiC epitaxy on commercial conductive 4H-SiC substrates and epitaxial 3C-SiC on ubiquitous Silicon substrates. These are not standard GaN platforms, but are standard for high power SiC devices. We have successfully integrated a bespoke chemical delivery system into the SiC epitaxy reactor at Warwick and explored chemical reactions with fundamental material parameters. Alongside this, test structures have been fabricated by co-implantation of vanadium and nitrogen. Both of these activities have shown insulating material in 4H-SiC and unexpectedly world record low contact resistances at the same time. This is counterintuitive, but if accurate, is an exiting development to improve both on and off state efficiency in a device which are normally subject to application specific trade offs.

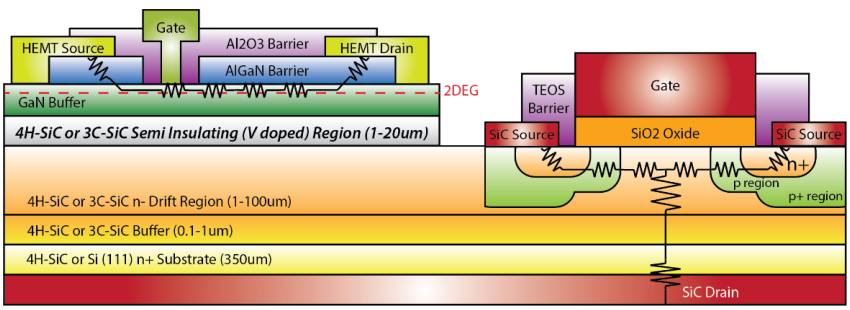




Fabricated test structures to test critical parameters of the insulating layer.

Relevance to manufacturing: This project introduces Silicon Carbide epitaxy to the CS Hub's portfolio, a strategic opportunity to integrate and explore how SiC and GaN can be used in different areas and concurrently.

Companies such as STMicroelectonics (Italy), Infineon (Austria), Wolfspeed (USA) and Denso (Japan) have recently secured SiC only fabrication lines for power device fabrication. With the recent UK addition to these SiC supply chains through the £17M APC project ESCAPE (End-to-end Supply Chain development for Automotive Power Electronics), this project has allowed interaction between the CS Hub, CS connected cluster with SiC power electronics and is projected to contribute significant value.



The proposed platform (GREY), with a GaN HEMT and SiC MOSFET co-located next to each other.

KEY PERFORMANCE INDICATORS

Annual and long-term targets to measure success

The CS Hub has a number of targets formed of measurable research outputs that are carefully designed to measure the success of the Hub in the context of the CS research environment. Many of these targets are only possible to achieve in the long-term, while others can demonstrate more immediate success for the Hub. The Key performance indicators (KPIs) for the Hub are detailed below. The following page contains some of the Hub's key achievements for these KPIs.

KPI	Success criteria
New industrial partners, based on exciting manufacturing challenges	5 per annum
New universities joining	5
Close collaborative links with other EPSRC Manufacturing Hubs and the EPSRC Centre for III-V Technology	Joint activities / events
Close collaborative links between the hub and major complementary overseas centres of excellence such as MIT, IMEC or NTU Singapore	2 over duration of Hub
Compound Semiconductor training centre activities to include: a) university and industry funded doctoral level training, b) MSc courses c) on-job and/or apprenticeship training to support industry d) summer schools for postdocs and PhD students	Delivery of a number of training activities per annum
Research and industrial awards per year for associated activity	Average of £5.5M (100% FEC) per annum
Conference presentations per year	Average of 10 per annum
Publications per year	Average of 20 per annum
Commercial impact activity to include: a) Number of IP disclosures/patents filed. b) Number of IP licences granted. c) Amount of VC funding generated, based on Hub technologies. d) New product roll-outs from partners, based upon Hub technologies. e) Sales value enabled by Hub technologies.	This is a late/lagging indicator and can be used later in the project to monitor success.
Outreach activity to include training	Delivery of a number of outreach activities per annum
Career development of Hub staff	Demonstration of staff development via securing fellowships, career training, etc.

THE HUB IN NUMBERS

Based on our Key Performance Indicators, and some other important measures of success, we have generated some impressive numbers at the Future CS Hub.

111 Publications

Conference presentations & abstracts **169**

75 Collaborations & partnerships

An additional 10 are currently in negotiation

Further funding **43**

Including 5 new awards.

46 Outreach & engagement

Including industrial events, international seminars and conferences.

Training activity **28**

8 Impact

Including 1 spin off company and 7 patent applications.

Career development **14**

27 Links to other hubs and centres overseas

STEM Ambassadors

We hope to see increasing opportunities for face-to-face outreach activity over the coming year. The Hub has begun coordinating with our cluster partners to train Hub researchers as STEM ambassadors, with a focus on working with schools at different key stages to promote the importance of compound semiconductors and related careers. Our researchers have also worked with Science Made Simple to develop engaging outreach content for key audiences and we plan to expand this work and enable researchers to further develop their communications skills.

Hub engagement with Industry

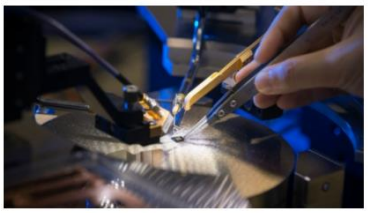
Over the past year we have continued to work with our industry partners in several ways and in accordance with TRL evolution of the Hub's work. This includes engaging with key partners such as the Welsh Assembly Government; industry partners providing PhD sponsorship for Hub students; and strategic partnerships to support specific elements of Hub research with companies such as Renishaw and TWI.

As described on page 15, the Hub and CSA Catapult recently hosted an interactive online workshop, exploring the challenges and added value of advanced (packaging) semiconductor integration. Also described above are the skills and research surveys the Hub developed to gain insight to industry challenges and needs,

Hub Website and Twitter

The content and structure of the Hub website (http:/compoundsemiconductorhub.org) has been updated over the last year and now includes several new areas to make content and Hub services more accessible. Twitter remains a key communication channel for the Hub (@FutureCSHub) and we now how have over 441 followers. We effectively use Twitter to promote Hub news and interact with audiences for events such as SIOE (described further on page 42).

About The Hub



Hub Research

Latest Hub News

Hub videos

The Hub has begun planning the production of a series of vidoes which will introduce the Hub and our research to key audiences. They will also focus on the Hub's work with industry partners and be an important resource to support our outreach work.

Conferences

The Hub was represented at the Photonics West Conference 2021 and In March 2021, the Semiconductor and Integrated Optoelectronics Conference (SIOE) took place. The conference was successfully translated into an online conference for the first time and attended by over 260 delegates (described further on page 42).

Training

The Hub has adapted its approach to learning and development over the las year and developed and delivered a series of online seminars on a range of topics, for example RF Theory and III-V MBE growth. The training has been delivered by a combination of external colleagues and Hub researchers and has spread expertise and good practice across the Hub. In total 13 sessions have been delivered and attended by over 30 Hub staff and students.

Hub Newsletter

The Hub issued a newsletter at the end of 2020 and will continue to share an updated version with audiences every 6 months. As well as providing updates on Hub news, the newsletter also includes a section focusing on a specific area of Hub research and spotlights recent publications.

December 2020

CS HUB NEWSLETTER

CS Hub

Engineering and Physical Sciences Research Council

Welcome to our new newsletter!

It has been a while since our last newsletter and given the challenges COVID has presented, we are keen to communicate with our industry and academic partners.

We will be circulating our newsletter every 6 months, sharing key Hub news and developments, and focusing on specific Hub research addressing long-term CS challenges.

As the Hub moves beyond the halfway stage of our 7-year research programme, we continue to work with over 30 industry partners and over 10 academic institutions to shape and drive forward our research.

Through this newsletter, our website and Twitter feed, and Hub events we will continue to update you on the Hub's progress and encourage you to contact us to discuss the Hub's research and any opportunities for collaboration.

SIOE Conference 2021

The Semiconductor and Integrated Opto-Electronics (SIOE) Conference will take place from the 30th March to 1st April 2021. This year's conference will be online, and we hope this will provide an opportunity for new areas of engagement. We will share more information and the agenda for the conference over the coming weeks.

Round 3 of Feasibility Studies Begin

The Hub funded 4 new feasibility studies, as part of a joint call with the Metrology, Photonics and Composites Manufacturing Hubs, with the 6-month studies starting in April 2020. Studies are being led by Bath, Cardiff (with Huddersfield and UCL), Sheffield, Strathclyde and Warwick Universities and further information on the studies and the research of the Hub can be found on our website.

National Epitaxy Facility Statement of Need

Members of the CS Hub recently joined academics from across the UK and took part in engaging discussions as part of the National Epitaxy Facility Statement of Need Community Consultation meeting. The Hub looks forward to engaging with the next steps of the process.

Hub skills and research surveys

The Hub has developed surveys to better understand the skills and recruitment needs CS manufacturing employers and to understand the areas of CS research that are of most interest to our industry partners. We would be grateful if you could take a few minutes to complete the skills and research surveys to help us with this.

Stay in Touch

All our latest news is available on our website:
compoundsemiconductorhub.org

Follow us on Twitter: @FutureCSHub

CS Hub Newsletter | December 2020

In Focus: Work Package 4

Research Summary

Recently, researchers from UCL and Cardiff University have demonstrated high performance telecommunication wavelength III-V semiconductor lasers monolithically grown on Si substrate for Si for realising a highly efficient on-chip light source in Si photonics. The results are published in *Advanced Optical Materials, Optics Letter, Journal of Physics D: Applied Physics, Journal of Selected Topics in Quantum Electronics*. The work covers material specification to industrial level device characterization and has significantly pushed forward the commercialisation of Si-based on-chip light source.

Progress and challenges to date

Inversion boundary, or so-called antiphase boundary, is a type of defect due to the polar on non-polar epitaxial growth, which makes it almost impossible to produce high-quality III-V devices on Si platform. The conventional method to solve this fundamental issue is using MOCVD system to fabricate bi-atomic Si steps, however, it is not compatible for MBE system and the fabrication of high performance QD laser.

Researchers demonstrated a novel technique by growing periodic straight and meandering single atomic steps to successfully confine the IB's propagation by only using MBE system. This result leads to the demonstration of high operating temperature QD laser based on Si platform.

"Our method of creating an APB-free GaAs/Si platform has solved the fundamental problem of high performance and CMOS-compatible Si-based on-chip light source by using molecular beam epitaxy system. This work has made all MBE-grown quantum dot laser on Si is highly viable solution for Si photonics"

Lead: Dr Mingchu Tang

Publication Spotlight

The papers listed below are some highlighted publications from recent months:

Preferred growth direction of III–V nanowires on differently oriented Si substrates Haotian Zeng *et al* 2020 *Nanotechnology* **31** 475708; DOI: 10.1088/1361-6528/abafd7

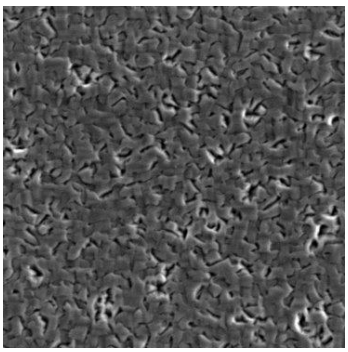
All-MBE grown InAs/GaAs quantum dot lasers with thin Ge buffer layer on Si substrates Junjie Yang *et al* 2021 *J. Phys. D: Appl. Phys.* **54** 035103; DOI: 10.1088/1361-6463/abbb49

Monolithic InP Quantum Dot Mode-Locked Lasers Emitting at 730 nm Zhibo Li *et al* 2020 *IEEE Photonics Technology Letters* **32** 1-1 DOI: 10.1109/LPT.2020.3012568

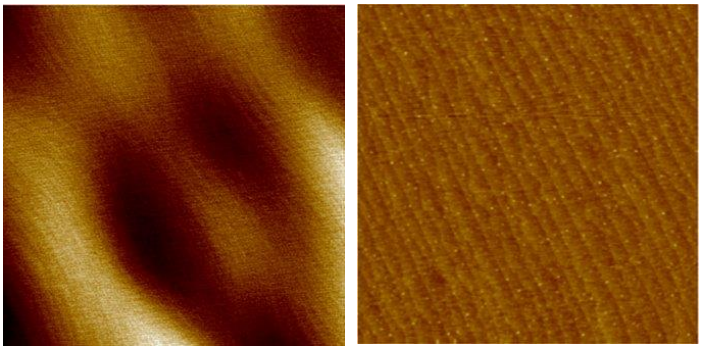
Influence of micro-patterning of the growth template on defect reduction and optical properties of non-polar (1120) GaN Jochen Bruckbauer *et al* 2021 *J. Phys. D: Appl. Phys.* **54** 025107; DOI: 10.1088/1361-6463/abbc37

Annihilation of antiphase boundary in GaAs layer grown on on-axis Si substrate

The heteroepitaxial growth of III-V polar material on group-IV non-polar material has been challenge for the realisation of monolithically integrated Si-based photonic integrated circuits. Due to the material dissimilarity, not only high density of threading dislocation are generated at the III-V/VI interface, but also high volume of two-dimensional defect, called antiphase boundaries (APB) raised which destroy the material quality significantly. The conventional method to overcome the APB issue is using the offcut Si substrate to create a bi-atomic Si step to avoid the formation of APBs. However, the use of offcut substrate cannot be widely used in the Si foundry for massive production. Recently, researchers have developed a method to realise a bi-atomic Si steps in metal-organic chemical vapour deposition system, but for the ideal platform for quantum dot (QD) Growth, molecular beam epitaxy (MBE), there is still lack of a sufficient solution yet to eliminate the APBs.

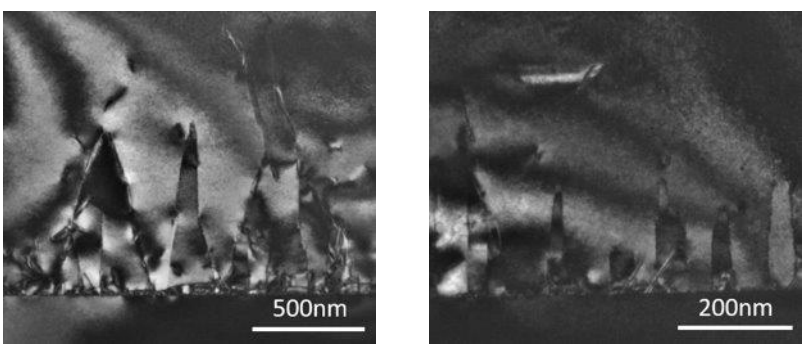


high density APBs behaving as cracks on the epi-surface



The Si surface with a random atomic step (left) and ordered single atomic step (right).

Led by University College London, and working together with University of Warwick and University of Cardiff, researchers in the first time, successfully investigate the APB generation, propagation and annihilation in the GaAs layer grown on on-axis Si substrate by using MBE system. The work has been published on the journal Advanced Optical Materials (DOI: 10.1002/adom.202000970). The APBs are nucleated at the interface of GaAs/Si and propagated freely into the following epi-layers without a sufficient annihilation, as shown in the Figure 1. To understand the reason of APB propagation, the researchers measure the Si wafer surface after the deoxidation, which shows a random step order due to the thermal equilibrium during the high temperature deoxidation process (~1000 ℃). To annihilate the APBS completely, a thin layer of high quality Si on the Si wafer has been grown in the MBE system which create a ordered single atomic step. Furthermore, despite the APBs are generated at the edge of Si single atomic steps, they are well-confined within the z-direction and annihilated by forming a closed loop with the increased growth temperature and thickness. epitaxy system. This work has made all MBE grown QD laser on Si is a highly viable solution for Si photonics.



The APBs are nucleated at the interface of GaAs/Si and propagate freely into the layers (left). With the help of ordered single atomic step, the APBs are well confined and formed closed loop.

Active & Passive Waveguides

Low-loss III-V waveguides (WGs) used as optical interconnects could provide the advantage of monolithic integration with active photonic components. However, most single-mode GaAs WGs have high propagation losses due to the relatively weak vertical refractive index contrast. Selective oxidation of high Al containing AlGaAs layers between the WG lower cladding and substrate could be a solution. This method allows for both active and passive components to be integrated on the same as-grown material without the need to increase the thickness of the epitaxial design.

We have designed both active and passive GaAs/AlGaAs structures, grown by UCL via MBE, that contain a 98% AlGaAs digital alloy (DA) layer to allow for this selective oxidation. Low-index AlO_x is formed by wet thermal oxidation using a humid H2/N2 forming gas in an Aloxtec (AET) 6" furnace. Development of the selective oxidation of this buried DA layer was required to understand the key parameters and limitations of the process, including delamination.

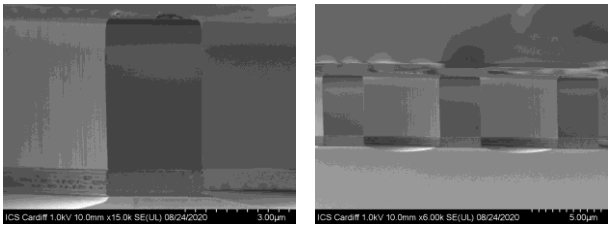


Figure 1 (above): SEM images of etched passive GaAs/AlGaAs spiral WGs, 5.6 µm in height, and the AlO_x layers formed via oxidation just above the substrate.

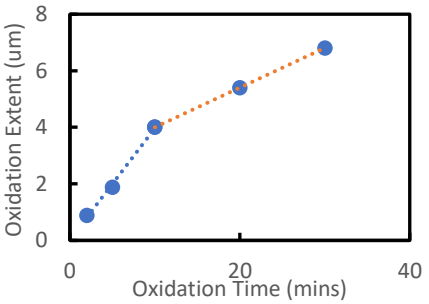


Figure 2 (left): Two clear regimes in the oxidation rate of the DA, at 400 degrees and 700 mbar, in the structure shown in figure 1.

Development of passive and active polymer based optical materials for high data rate WG routing and interconnects has gained increased attention because of their excellent properties such as low absorption, cost savings, and ease in fabrication. However, optical polymers are typically limited in the range of their refractive indices. Combining polymeric and inorganic optical materials provides advantages for development of composites with higher refractive indices.

Complex structures have been developed where BCB and SU-8 form the polymer portion, and Ta_2O_5 and SiO_2 the inorganic. We have developed and characterised Ta2O5 films grown by ALD (figure 3) on GaAs, SiO_2, and on a structure similar to that in figure 4.

Ta_2O_5 has been chosen for its high refractive index at 1.3 µm, with a refractive index of 2.08 achieved with the stack in figure 4 after characterisation of table temperature effect and growth per cycle. Alongside the ALD, thin film measurement capabilities have been increased with further work undertaken on the ellipsometer purchased using the CSHub underpinning equipment award from EPSRC. This has allowed for non-destructive measurements of multi-layer thin film structures.

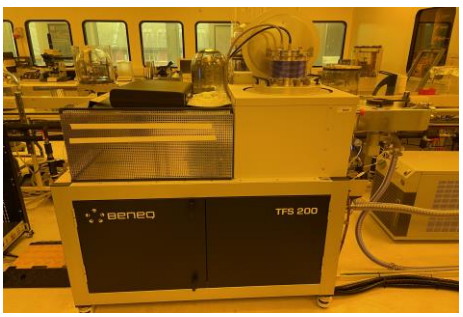


Figure 3: Beneq ALD with 8" capability in ICS cleanroom at Cardiff University.

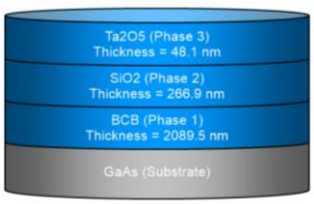


Figure 4 (above): An example of a polymer-inorganic WG structure.

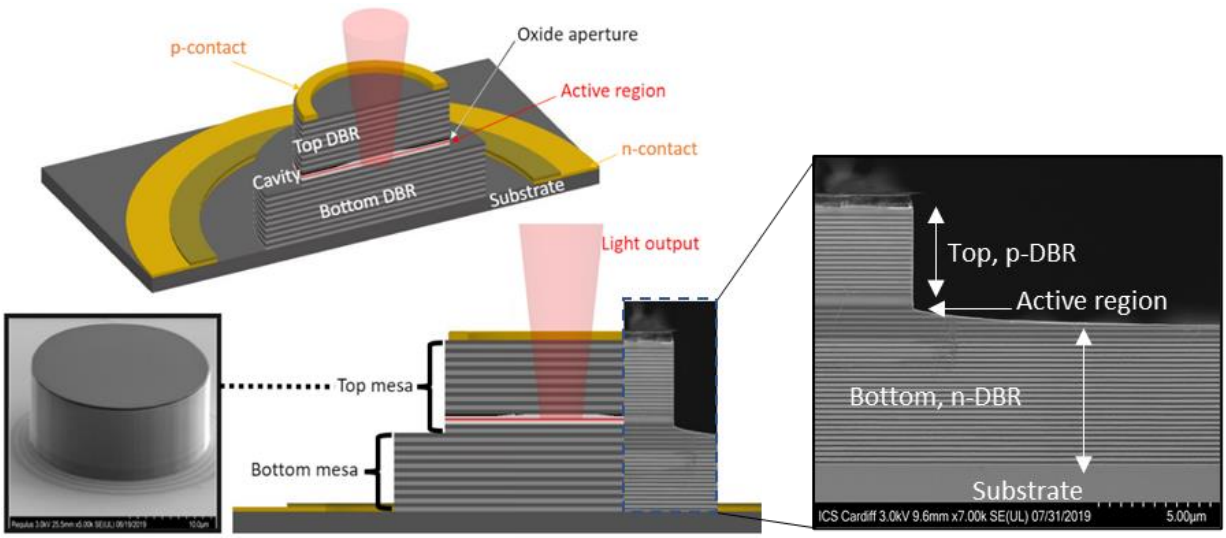
NEW AWARD HIGHLIGHT: ATLAS

Advanced Manufacturing Techniques for Semiconductor LASers

The ATLAS project (Advanced Manufacturing Techniques for Semiconductor LASers) is a Smart Expertise Award from Business Wales within the Welsh Government. It is a key project for the future of the compound semiconductor industry in Wales and is 50 percent funded by the SMART Expertise programme and 50 percent from industry partners, these being the Compound Semiconductor Centre, IQE Plc, SPTS Technologies, and Rockley Photonics.

ATLAS provides an opportunity to further link University research with industry to develop next generation technologies, tackling many of the current challenges faced by today's manufacturers. Dr Samuel Shutts explains the award will "support collaborative projects between industry and Welsh research organisations which address industrial challenges, focusing on commercialisation of new products, processes or services and growth in capacity and capability'. Sam continued "ATLAS is an industry-focused project with an objective to enhance the manufacturing capability of compound semiconductor (CS) lasers, putting South Wales at the leading-edge of CS laser production".

The project will develop key processes to be scaled-up by industry, enabling next generation data communications, for example high-definition streaming and 5G connectivity; and sensing capabilities, for example the face/gesture recognition capability of digital devices or the electronic systems that assist drivers in driving and parking cars.



Both data communication and sensing are technologies that rely on two types of CS laser devices (vertical-cavity surface-emitting lasers, and edge-emitting lasers). ATLAS will focus on the development and production of these lasers, with the key aim being to allow low-cost, energy efficient manufacturing in high-volume production. Such internationally leading advances in CS lasers are excitingly set to benefit both science and industry.

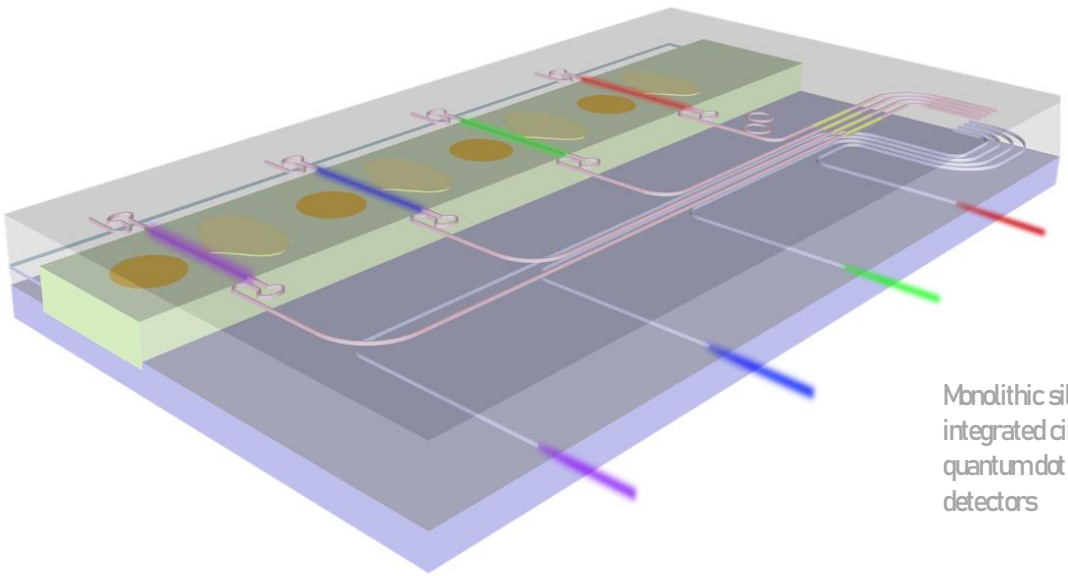
NEW AWARD HIGHLIGHT: QUDOS

Quantum Dots on Silicon

The QUDOS programme (Quantum Dots on Silicon) will investigate new ways of integrating all the parts that are needed for high capacity optical communications and signal processing on a single silicon chip. Researchers from UCL's Photonics Group, with collaborators from Cambridge, Cardiff and Southampton Universities, have been awarded a five year UKRI-EPSRC Programme Grant to create the first optical integrated circuits on silicon with monolithically integrated quantum dot laser sources.

The sensing, processing and transport of information is at the heart of modern life, as can be seen from the ubiquity of smart-phone usage on any street. The internet depends on optical systems from fibre to the home, through data centres to the trans-oceanic optical cables that link the nations of the earth. Creating these systems requires the mechanical alignment of components to accuracies of less than a micron, about one hundredth of the diameter of a human hair, a costly and labour intensive process.

The QUDOS research team have invented technologies to integrate the required components on silicon chips in the same manner as electronic systems are now realised as integrated circuits, making possible the first data interconnects, switches and sensors that use lasers monolithically integrated on silicon. QUDOS offers the potential to transform Information and Communication Technology (ICT) by changing fundamentally the way in which data is sensed, transferred between and processed on silicon chips.



Monolithic silicon optical integrated circuit including quantum dot lasers and detectors

The QUDOS programme builds on previous work by team members which demonstrated the world's first successful telecommunications wavelength lasers directly integrated on silicon substrates. Removing the need to assemble individual components will enable vastly increased scale and functionality for information systems at greatly reduced cost.

Professor Alwyn Seeds, Principal Investigator for QUDOS, added "The QUDOS Programme, through the monolithic integration of all required optical ICT functions on silicon, will have a similar transformative effect on ICT to that which the creation of the first silicon integrated electronic circuits had on electronics."

Overview

Following the cancellation of the Semiconductor and Integrated OptoElectronics Conference (SIOE) in 2020, the Hub was determined to deliver SIOE in 2021.

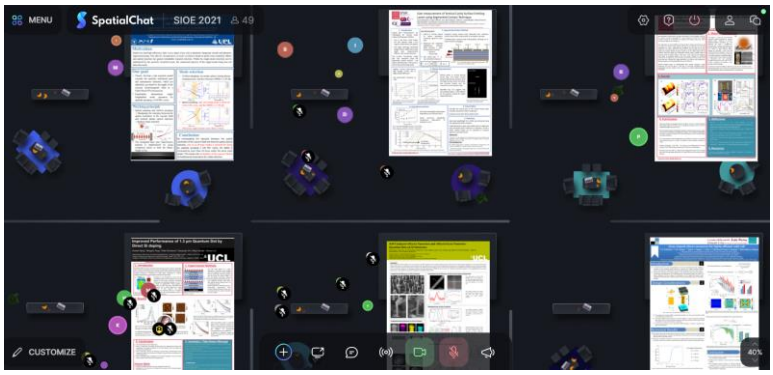
Through careful choice in online tools, the 34th SIOE conference was successfully translated into an exciting online programme. This meant that over three days, over 260 delegates could enjoy live talks on a wide range of topics from invited international speakers with opportunities for collaboration and communication. Across the conference, over 80 oral presentations covered a wide range of expertise, including: Materials Development and the impact of materials innovations on devices; New Approaches for Datacom/Telecom Wavelength Lasers; Lasers and Laser Systems; Compound Semiconductor Devices on Silicon; Detectors and Related Materials; Modulators and Modulation.

We were delighted to welcome two invited speakers. Professor Weng Chow from Sandia National Laboratories in Albuquerque, New Mexico delivered a thought-provoking talk on p-doping in quantum dot lasers, summarising recent work on Quantum Dot laser modelling and design. Professor Asa Haglund from Chalmers University of Technology, Göteborg delivered a fantastic talk on very short wavelength VCSELs and light emitters.

Left: Professor Weng Chow from Sandia National Laboratories in Albuquerque. Right: Professor Asa Haglund from Chalmers University of Technology, Göteborg

Poster and careers session

To ensure SIOE 2021 did not lack the interactive element so important to academic exchange, SIOE utilised the platform Spatial Chat for poster presentations, allowing delegates to interact and talk with poster presenters, other delegates and to make new connections. Not only did spatial offer opportunity to network and connect with new colleagues, but the platform was also the venue for a careers session supported by the CS Hub and CS Cluster, focusing on Compound Semiconductor careers including current job opportunities in South Wales and beyond.



Left: one of the interactive poster sessions that took place during SIOE

Below: SIOE again received generous sponsorship from our partners

IOP Institute of Physics
Quantum Electronics and Photonics Group

IOP Institute of Physics
Semiconductor Physics Group

RESEARCH OUTPUT: PUBLICATIONS

Peer reviewed publications are a key indicator of our research success

- 1.3 μm InAs/GaAs quantum dot lasers on silicon with GaInP upper cladding layers. Wang J, Hu H, Yin H, et al. Photonics Research. 2018:6 (4); pp 321-325. DOI: 10.1364/PRJ.6.000321
- 3D ITO-nanowire networks as transparent electrode for all-terrain substrate. Li Q, Tian Z, Zhang Y, et al. Scientific Reports 9, 4983 (2019). DOI: 0.1038/s41598-019-41579-2.
- A direct epitaxial approach to achieving ultra-small and ultra-bright InGaN-based micro light emitting diodes (μLEDs). J. Bai, Y. Cai, P. Feng, et al. ACS Photonics 7, 411-415 (2020); DOI: acsphotonics.9b01351
- A real time high sensitivity high spatial resolution quantum well hall effect magnetovision camera. Balaban E, Ahmad E, Zhang Z, et al. Sensors and Actuators A: Physical. 2017:265, pp 127-137. DOI: 10.1016/J.SNA.2017.08.035
- Achieving wavelength emission beyond the C-band from Type-II InAs-GaAsSb quantum dots grown monolithically on silicon substrate. Salhi A, Alshaibani S, Alaskar Y, et al. Journal of Alloys and Compounds, 771, pp 382-386, 2019. DOI: 10.1016/j.jallcom.2018.08.276.
- All-MBE grown InAs/GaAs quantum dot lasers with thin Ge buffer layeron Si substrates. Yang J, Liu Z et al, Journal of Physics. D: Applied Physics, 54 035103, 2021 DOI: 10.1088/1361-6463/abbb49
- Altering the Optical Properties of GaAsSb-Capped InAs Quantum Dots by Means of InAlAs Interlayers. Salhi A, Alshaibani S, Alaskar Y et al. Nanoscale Research Letters, 14:41, 2019. DOI: 10.1186/s11671-019-2877-2.
- Buffer induced current-collapse in GaN HEMTs on Highly Resistive Si Substrates. Chandrasekar H, Uren M.J, Eblabla A, et al. IEEE Electron Device Letters. 2018:39(10), pp 1556-1559. DOI: 10.1109/LED.2018.2864562
- Cathodoluminescence studies of chevron features in semi-polar (112-2) InGaN/GaN multiple quantum well structures. Brasser C, Bruckbauer J, Gong Y. P et al. Journal of Applied Physics. 123, 174502 (2018). DOI: 10.1063/1.5021883.
- CMOS-compatible multi-band plasmonic TE-pass polarizer. Abadia N, Ghulam Saber M.D, Bello F et al. Optics Express. 2018:26(23), pp 30292-30304. DOI: 10.1364/OE.26.030292.
- Confocal photoluminescence investigation to identify basal stacking fault's role in the optical properties of semi-polar InGaN/GaN lighting emitting diodes. Zhang Y, Smith R.M, Jiu L et al. Scientific Reports 9, 9735 (2019). DOI: 10.1038/s41598-019-46292-8.
- Continuous-Wave Quantum Dot Photonic Crystal Lasers Grown on On-axis Si (001). Zhou T, Tang M, Xiang G, et al. Nature Communications 11, 977 (2020). DOI: 10.1038/s41467-020-14736-9

- Controllable Uniform Green Light Emitters Enabled by Circular HEMT-LED Devices. Cai Y, Gong Y, Bai J, et al. IEEE Photonics Journal. 2018:10(5). DOI: 10.1109/JPHOT.2018.2867821
- Degradation of III-V Quantum Dot Lasers Grown directly on Silicon substrates. Shutts S, Allford C.P, Spinnier C et al. IEEE Journal of Selected Topics in Quantum Electronics, 25, 6. DOI: 10.1109/JSTQE.2019.2915994
- Demonstration of InAs/InGaAs/GaAs Quantum Dots-in-a-Well Mid-Wave Infrared Photodetectors Grown on Silicon Substrate. Chen W, Deng Z, Guo D, et al. Journal of Lightwave Technology. 2018:36, 2572. DOI 10.1109/JLT.2018.2811388
- Demonstration of Si based InAs/GaSb type-II superlattice p-i-n photodetector. Deng Z, Guo D, Burguete C.G, et al. Infrared Physics & Technology, 101, (2019), pp 133-137. DOI: 10.1016/j.infrared.2019.06.011.
- Designing tomorrow's VCSELs. Shutts S and Gallagher D. CS Magazine Vol. 26, issue 4, June 2020
- Determination of Preferred Growth Direction of III-V Nanowires on Differently Oriented Si Substrate. H. Zeng, X. Yu, et al. Nanotechnology 31, 475708 (2020) DOI: 10.1088/1361-6528/abafd7
- Determining GaN nanowire polarity and its influence on light emission in the scanning electron microscope. Naresh-Kumar G, Bruckbauer J, Winkelmann A, et al. Nano Lett. 19, 3863(2019). DOI: 10.1021/acs.nanolett.9b01054.
- Development and Optimisation of Low Power Magnetic Flux Leakage Inspection Parameters for Mild Steel Welds. Watson J.M, Liang C.M, et al. Insight, Nov 2020, G421:M421
- Droplet manipulation and horizontal growth of high-quality self-catalysed GaAsP nanowires. Zhang Y, et al. Nano Today 34, 100921, 2020 DOI: 10.1016/j.nantod.2020.100921
- Effect of rapid thermal annealing on threading dislocation density in III-V epilayers monolithically grown on Silicon. Li W, Chen S, Tang M, et al. Journal of Applied Physics, 2018:123(21); 215303. DOI: 10.1063/1.5011161
- Efficient Light Down-Conversion via Resonant Energy Transfer in InGaN Nanohole Arrays Coated by Lead Halide Perovskite Nanocrystals. ACS Applied Nano Mater. 3, 2167-2175 (2020); DOI: 10.1021/acsanm.9b02154
- Electrically Injected Hybrid Organic/Inorganic III-Nitride White Light-Emitting Diodes with Nonradiative Förster Resonance Energy Transfer. Ghataora S, Smith R.M, Athanasiou M, Wang T. ACS Photonics. 2017:5(2), pp 642-647. DOI: 10.1021/acsphotonics.7b01291

- Electrically pumped continuous-wave 1.3 μm InAs/GaAs quantum dot lasers monolithically grown on on-axis Si (001) substrates. Chen S, Liao M, Tang M, et al. Optics Express, 2017:25(5), pp 4632-4639. DOI: 10.1364/OE.25.004632
- Electrically pumped continuous-wave O-band quantum-dot superluminescent diode on silicon. Lu Y, et al. Optics Letters 45 (19), 5468-5471, 2020. DOI: 10.1364/OL.401042
- Elevated temperature lasing from injection microdisk lasers on silicon. Kryzhanovskaya N.V, Moiseev E.I, Polubavkina Y.S, et al. Laser Physics Letters 2017:15(1), pp 015802. DOI: 10.1088/1612-202X/aa9306
- Evolution of the luminescence in non-polar (11-20) GaN overgrown on a progression of different GaN microstructures. Bruckbauer J, Gong Y, et al. Journal of Physics D: Applied Physics, 54, 025107, 2021
- Explore an approach towards the intrinsic limits of GaN electronics. Jiang S, Cai Y, Feng P, et al. ACS Appl. Mater. Interfaces, 12, 12949−12954 (2020); DOI: 10.1021/acsami.9b19697
- Flexibility of Ga-containing Type-II superlattice for long-wavelength infrared detection. Delmas M; Kwan D.C.M; Debnath M.C, et al. Journal of Physics D: Applied Physics, 52, 47. DOI: 10.1088/1361-6463/ab3b6a.
- Gain switching of monolithic 1.3 um InAs/GaAs quantum dot lasers on silicon. Hantschmann C, Vasil'ev P.P, Chen S, et al. Journal of Lightwave Technology, 2018:36(18), pp 3837-2842. DOI: 10.1109/jlt.2018.2851918
- Gain Switching of Monolithic 1.3 μm InAs/GaAs Quantum Dot Lasers on Silicon. Hantschmann C, Vasil'ev P.P, Chen S, et al. Journal of Lightwave Technology, vol. 36, no. 18, pp. 3837-3842, Sept, 2018. DOI: 10.1109/JLT.2018.2851918
- Growth mechanisms for InAs/GaAs QDs with and without Bi surfactants. Chen X.Y, Gu Y, Ma Y.J, et al. Materials Research Express 6 (1), 015046 (2018). DOI: 10.1088/1555-6611/aae194.
- Heat-sink free CW operation of injection microdisk lasers grown on Si substrate with emission wavelength beyond 1.3 μm. Kryzhanovskaya N, Moiseev E, Polubavkina Y, et al. Optics Letters, 2017:42(17), pp 3319-3322. DOI :10.1364/OL.42.003319
- Heavily tin-doped indium oxide nano-pyramids as high-performance gas sensor. Li Q, Zhang Y, Feng L, et al AIP Advances 8, 115316 (2018). DOI: 10.1063/1.5048622.

- Heterostructure and Q-factor engineering for low-threshold and persistent nanowire lasing. Skalsky S, Zhang Y., Alanis J.A, et al. Light: Science & Applications 9, 43 (2020). DOI: 10.1038/s41377-020-0279-y
- High Detectivity and Transparent Few-Layer MoS2/Glassy-Graphene Heterostructure Photodetectors. Xu H, Han X, Dai X, et al. Advanced Mater. 2018:30(13), 1706561. DOI: 10.1002/adma.201706561
- High Modulation Bandwidth of Semi-polar (11-22) InGaN/GaN LEDs with Long Wavelength Emission. Haggar J, Cai Y, Ghataora S.S et al. ACS, 2020, DOI: acsaelm.0c00399
- III–V quantum-dot lasers monolithically grown on silicon. Liao M, Chen S, Park J, et al. Semiconductor Science and Technology. 2018:33(12), 3002. DOI: 10.1364/OFC.2019.W4E.1.
- Imaging basal plane stacking faults and dislocations in (11-22) GaN using electron channelling contrast imaging. Naresh-Kumar G, Thomson D, Zhang Y, et al. Journal of Applied Physics, 124, 065301 (2018). DOI: 10.1063/1.5042515.
- Increasing maximum gain in InAs quantum dot lasers on GaAs and Si. Shutts S, Spinnler C, Li Z, et al. DOI: 10.1109/IPCon.2018.8527302
- Indium tin oxide nanowires grown on Ni foam as voltage self-stabilizing supercapacitor electrode. Li Q, Wang Z, Zhang Y, et al. Journal of Materials Research. 2019:34(18), pp 3195-3203. DOI: 10.1557/jmr.2019.241
- Influence of MOVPE environment on the selective area thermal etching of GaN nanohole arrays. Coulon P-M, Feng P, Damilano B, et al. Scientific Reports 10, 5642 (2020); DOI: s41598-020-62539-1
- InGaAs/AlAs Resonant Tunneling Diodes for THz Applications: An Experimental Investigation. Muttlak S.G, Abdulwahid O. S, Sexton J et al. IEEE Journal of the Electron Devices Society, 6, pp 254-262, 2018. DOI: 10.1109/JEDS.2018.2797951.
- InGaAs/AlAs/GaAs metamorphic asymmetric spacer layer tunnel (mASPAT) diodes for microwaves and millimeter-waves detection. Salhi, J. Sexton, et al. Journal of Applied Physics 127, 194505, 2020 DOI: 10.1109/UCMMT47867.2019.9008328
- Integrating III-V quantum dot lasers on silicon substrates for silicon photonics. Liao M, Chen S, Tang M, et al. Silicon Photonics XII, 2017, 10108; DOI: 10.1117/12.2249761
- Integration of III-V lasers on Si for Si photonics. Tang M, Park J-S, Wang Z, et al. Progress in Quantum Electronics. 2019:66, pp 1-18. DOI 10.1016/j.pquantelec.2019.05.002

- Inversion Boundary Annihilation in GaAs Monolithically Grown on On-Axis Silicon (001). Li K et al, Advanced Optical Materials, 2000970 (2020) DOI: 10.1002/adom.202000970
- Investigation of growth parameters influence on self-catalyzed ITO nanowires by high RF-power sputtering. Li Q, Zhang Y, Feng L, et al. Nanotechnology. 2018:29(16). DOI: 10.1088/1361-6528/aaafa7
- Investigation of the influence of an InGaN superlattice prelayer on the performance of semi-polar (11-22) green LEDs grown on silicon (113) substrates. Zhao X, Huang K, Bruckbauer J, et al. Scientific Reports 10, 12650 (2020) DOI: s41598-020-69609-4
- Investigations of Asymmetric Spacer Tunnel Layer Diodes for High-Frequency Applications. Zainul Ariffin K.N, Wang Y, Abdullah M.R.R, et al. IEEE Transactions on Electron Devices 2018:65(1), pp 64-71. DOI: 10.1109/TED.2017.2777803
- ITO nanowires grown on Ni foam as voltage self-stabilizing supercapacitor electrode. Li Q, Wang Z, Zhang Y, et al. Journal of Materials Research 34, 3195-3203 (2019). DOI: 10.1557/jmr.2019.241
- Low-cost InP–InGaAs PIN–HBT-based OEIC for up to 20 Gb/s optical communication systems. Muttlak S G, Kostakis I, Abdulwahid O S ,et al. ET Optoelectronics, 13, 3, pp 144 – 150. DOI: 10.1049/iet-opt.2018.5032.
- Low-noise 1.3 μm InAs/GaAs quantum dot laser monolithically grown on silicon. Liao M, Chen S, Liu Z, et al. Photonics Research 6, 1062-1066 (2018). DOI: 10.1364/PRJ.6.001062
- Luminescence behaviour of semi-polar (10-11) InGaN/GaN 'bow-tie' structures on patterned Si substrates. Bruckbauer J, Trager-Cowan C, Hourahine B, et al. Journal of Applied Physics. 127, 035705 (2020). DOI:10.1063/1.5129049
- Magnetic field frequency optimisation for MFL imaging using QWHE sensors. I Watson J.M, Liang C.M, et al. Insight, 62(7). 2020
- Material and device characterization of Type-II InAs/GaSb superlattice infrared detectors. Delmas M, Debnath M.C, Liang B, et al. Infrared Physics & Technology. 2018:94, pp 286-290. DOI: 10.1016/j.infrared.2018.09.012
- Monolithic InP Quantum Dot Mode-Locked Lasers Emitting at 730 nm. Li Z, Allford C.P, et al. IEEE Photonics Technology Letter 2(17), 1073-1076 DOI: 10.1109/LPT.2020.3012568
- Monolithic multiple colour emission from InGaN grown on patterned non-polar GaN. Gong Y, Jiu L, Bruckbauer J, et al. Scientific Reports, 9, 986. (2019). DOI: 10.1038/s41598-018-37575-7.
- Monolithic non-polar (11-20) GaN metal-semiconductor-metal photo-detectors with superior performance on silicon. Cai Y, Shen S, Zhu C, et al. ACS Appl. Mater. Interfaces 12, 25031–25036 (2020). DOI:10.1021/acsami.0c04890

RESEARCH OUTPUT: PUBLICATIONS

- Monolithic quantum-dot distributed feedback laser array on silicon. Wang Y, Chen S, Yu Y, et al. Optica 2018:5(5), pp 528-533. DOI: 10.1364/OPTICA.5.000528
- Monolithically integrated multi-colour lasing from microdisk cavity from an InGaN / GaN MQWs On Si Substrate. Athanasiou M, Smith R, Pugh J, et al. Scientific Reports 7, 10086; (2017) DOI:10.1038/s41598-017-10712-4
- Monolithically integrated white light LEDs on (11-22) semi-polar GaN templates. Poyatzis N, Athanasiou M, Nai J, et al. Scientific Reports. 2019:9;986. DOI: 10.1038/s41598-018-37575-7
- Monolithically multi-color lasing from an InGaN microdisk on a Si substrate. Athanasiou M, Smith R.M, Pugh J, et al. Scientific Reports. 2017:7, 10086. DOI: 10.1038/s41598-017-10712-4
- Nanowire Quantum Dot Surface Engineering for High Temperature Single Photon Emission. Yu P, Li Z, Wu T, et al. ACS Nano. 2019:12(11), pp 13492 – 13500. DOI : 10.1021/acsnano.9b07204
- Non-polar (11-20) GaN grown on sapphire with double overgrowth on micro-rod/stripe templates. Bai J, et al. Semiconductor Science and Technology. 2018: 33; 12. DOI:10.1088/1361-6641/AAED93
- O-band InAs/GaAs quantum dot laser monolithically integrated on exact (001) Si substrate. Li K, Liu Z, Tang M, et al. Crystal Growth 2019. DOI: 10.1016/J.CRYSGRO.2019.01.016
- Optical and polarisation properties of nonpolar InGaN-based light-emitting diodes grown on micro-rod templates. Bai J, Jiu L, Fletcher P, et al. Scientific Reports 9, 9770 (2019) DOI: 10.1038/s41598-019-46343-0
- Optical polarization properties of (11-22) semi-polar InGaN LEDs with a wide spectral range. Poyiatzis N, Bai J, Smith R. M, et al. Scientific Reports 10, 7191 (2020); DOI: 10.1038/s41598-020-64196-w
- Optical Properties of Semi-polar (11-22) AlxGa1-xN with High Al Composition. Li Z, Wang L, Bruckbauer J, et al. Applied Physics Letters. 2017:10(9) 110, 082103. DOI: 10.1063/1.4977428
- Optimization of 1.3 μm InAs/GaAs quantum dot lasers epitaxially grown on silicon: taking the optical loss of metamorphic epilayers into account. Wang Y, Bai Y, Liu, H et al. Semiconductor Science and Technology. 33, 123002 (2018). DOI: 10.1088/1555-6611/aae194.
- Origin of defect tolerance in InAs/GaAs quantum dot lasers grown on silicon. Liu Z, Hantschmann C, Tang M et al. Journal of Lightwave Technology, June 2019, P 1-1. DOI: 10.1109/JLT.2019.2925598.
- Overgrowth and characterisation of (11-22) semipolar GaN on (113) silicon with a two-step method. Cai Y, Yu X, Zhao X, Jiu L, et al. Semiconductor Science and Technology. 2019:34(4). DOI: 10.1088/1361-6641/AB08BF

- Overgrowth and strain investigation of (11-20) non-polar GaN on patterned templates on sapphire. Jiu L, Gong Y, Wang T. Scientific Reports 8, 9898 (2018). DOI: 10.1038/s41598-018-28328-7.
- Photonic integration platform with pump free microfluidics. Thomas R, Harrison A, Barrow D, et al. Optics express, 2017:25(20), pp 23634-23644. DOI: 10.1364/OE.25.023634
- Physical modelling and experimental characterisation of InAlAs/InGaAs avalanche photodiode for 10 Gb/s data rates and higher. Abdulwahid OS, Sexton J, Kostakis I, et al. IET Optoelectronics. 2018:12(1), pp 5-10. DOI: 10.1049/iet-opt.2017.0068
- Physical modelling of InGaAs–InAlAs APD and PIN photodetectors for> 25 Gb/s data rate applications. Abdulwahid O. S, Kostakis I, Muttlak S.G et al. IET Optoelectronics 13 (1), 40-45, 2019. DOI: 10.1049/iet-opt.2018.5030
- Polarization-Independent Mode-Evolution-Based Coupler for the Silicon-on-Insulator Platform. Wang Y, Xu L, Yun H, et al. Photonics Journal (2018). DOI: 10.1109/JPHOT.2018.283576
- Polarized white light from hybrid organic/III-nitrides grating structures. Athanasiou M, Smith R. M, Ghataora S, et al. Scientific Reports 7, 39677. (2017) DOI: 10.1038/srep39677
- Porosity-enhanced solar powered hydrogen generation in GaN photoelectrodes. Hou Y, Ahmed Syed Z, Jiu L, et al. Appl. Phys. Lett. 111, 203901 (2017) DOI: 10.1063/1.5001938
- Recent progress in epitaxial growth of III–V quantum-dot lasers on silicon substrate. Pan S, Cao V, Liao M, et al. Journal of Semiconductors. 2019:40, 101302. DOI: 10.1088/1674-4926/40/10/101302
- Scanning electron microscope as a flexible tool for investigating the properties of UV-emitting nitride semiconductor thin films. Trager-Cowan C, Alasmari A, Avis W, et al. Phonics Research. 2019:7(11), pp B73 – B82. DOI: 10.1364/PRJ.7.000B73
- Selective area intermixing of III–V quantum-dot lasers grown on silicon with two wavelength lasing emissions. Liao M, Li W, Tang M et al. Semiconductor Science and Technology, 34, 8, (2019). DOI: 10.1088/1361-6641/ab2c24.
- Semi-polar (11-22) AlGaN on overgrown GaN on micro-rod templates: simultaneous management of crystal quality improvement and cracking issue. Zi Z, Jiu L, Wang L, et al. Applied Physics Letter. 2017:110(8), 082103 (2017). DOI: 10.1063/1.4977094
- Semi-polar (11-22) AlGaN on overgrown GaN on micro-rod templates: simultaneous management of crystal quality improvement and cracking issue. Li Z, Jiu L, Gong Y, et al. Applied Physics Letters. 110, 082103. (2017) DOI: 10.1063/1.4977094
- Semi-polar InGaN-based green light-emitting diodes grown on silicon. Shen S, Zhao X, Yu X, et al. Physica Status Solidi A. 2019: DOI: 10.1002/pssa.201900654

- Overgrowth and strain investigation of (11-20) non-polar GaN on patterned templates on sapphire. Jiu L, Gong Y, Wang T. Scientific Reports 8, 9898 (2018). DOI: 10.1038/s41598-018-28328-7.
- Photonic integration platform with pump free microfluidics. Thomas R, Harrison A, Barrow D, et al. Optics express, 2017:25(20), pp 23634-23644. DOI: 10.1364/OE.25.023634
- Physical modelling and experimental characterisation of InAlAs/InGaAs avalanche photodiode for 10 Gb/s data rates and higher. Abdulwahid OS, Sexton J, Kostakis I, et al. IET Optoelectronics. 2018:12(1), pp 5-10. DOI: 10.1049/iet-opt.2017.0068
- Physical modelling of InGaAs–InAlAs APD and PIN photodetectors for> 25 Gb/s data rate applications. Abdulwahid O. S, Kostakis I, Muttlak S.G et al. IET Optoelectronics 13 (1), 40-45, 2019. DOI: 10.1049/iet-opt.2018.5030
- Polarization-Independent Mode-Evolution-Based Coupler for the Silicon-on-Insulator Platform. Wang Y, Xu L, Yun H, et al. Photonics Journal (2018). DOI: 10.1109/JPHOT.2018.283576
- Polarized white light from hybrid organic/III-nitrides grating structures. Athanasiou M, Smith R. M, Ghataora S, et al. Scientific Reports 7, 39677. (2017) DOI: 10.1038/srep39677
- Porosity-enhanced solar powered hydrogen generation in GaN photoelectrodes. Hou Y, Ahmed Syed Z, Jiu L, et al. Appl. Phys. Lett. 111, 203901 (2017) DOI: 10.1063/1.5001938
- Recent progress in epitaxial growth of III–V quantum-dot lasers on silicon substrate. Pan S, Cao V, Liao M, et al. Journal of Semiconductors. 2019:40, 101302. DOI: 10.1088/1674-4926/40/10/101302
- Scanning electron microscope as a flexible tool for investigating the properties of UV-emitting nitride semiconductor thin films. Trager-Cowan C, Alasmari A, Avis W, et al. Phonics Research. 2019:7(11), pp B73 – B82. DOI: 10.1364/PRJ.7.000B73
- Selective area intermixing of III–V quantum-dot lasers grown on silicon with two wavelength lasing emissions. Liao M, Li W, Tang M et al. Semiconductor Science and Technology, 34, 8, (2019). DOI: 10.1088/1361-6641/ab2c24.
- Semi-polar (11-22) AlGaN on overgrown GaN on micro-rod templates: simultaneous management of crystal quality improvement and cracking issue. Zi Z, Jiu L, Wang L, et al. Applied Physics Letter. 2017:110(8), 082103 (2017). DOI: 10.1063/1.4977094
- Semi-polar (11-22) AlGaN on overgrown GaN on micro-rod templates: simultaneous management of crystal quality improvement and cracking issue. Li Z, Jiu L, Gong Y, et al. Applied Physics Letters. 110, 082103. (2017) DOI: 10.1063/1.4977094
- Semi-polar InGaN-based green light-emitting diodes grown on silicon. Shen S, Zhao X, Yu X, et al. Physica Status Solidi A. 2019: DOI: 10.1002/pssa.201900654

RESEARCH OUTPUT: PUBLICATIONS

- Ultra-low threshold InAs/GaAs quantum dot microdisklasers on planar on-axis Si (001) substrates. Zhou T, Tang M, Xiang G, et al. Optica. 2019:6(4), pp 430-435. DOI: 10.1364/OPTICA.6.000430
- Ultra-small, ultra-compact and ultra-high efficient InGaN micro light emitting diodes (μLEDs) with narrow spectra linewidth. Bai J, Cai Y, et al. ACS Nano 14, 6906-6911, 2020. DOI: 10.1021/acsnano.0c01180

Work package leads and investigators

Prof Peter Smowton is Hub Director and Head of School at the School of Physics and Astronomy, Cardiff University

Prof David Wallis is Platform Work Package 1 (Epitaxy) Lead and Professor of Compound Semiconductors at the School of Engineering, Cardiff University

Dr Sara-Jayne Gillgrass is Platform Work Package 2 (Fabrication) Lead and a Research Associate at the school of Physics and Astronomy, Cardiff University

Dr Craig Allford is Work Package 3 (Fast fabrication) Lead and is a Research Associate at the School of Physics and Astronomy, Cardiff University

Prof Huiyun Liu is Work Package 4 (Optoelectronic devices for data comms) Lead and Professor of Semiconductor Photonics at the Department of Electronic and Electrical Engineering, University College London

Prof Khaled Elgaid is Work Package 5 (RF Devices and MMICs) Lead and Professor at the School of Engineering, Cardiff University

Prof Tao Wang is Work Package 6 (LEDs and RF diodes) Lead and Professor of Advanced Optoelectronics at the Department of Electronic and Electrical Engineering, University of Sheffield

Prof Mo Missous, is Work Package 7 Lead at the School of Electrical and Electronic Engineering, the University of Manchester

Dr Nicolas Abadia is Work Package 9 Lead and Lecturer at the School of Physics and Astronomy, Cardiff University

Prof Alwyn Seeds is Professor of Opto-Electronics at the Department of Electronic and Electrical Engineering, UCL

Prof Paul Tasker is Professor at the School of Engineering, Cardiff University

Prof Sir Michael Pepper, is Pender Professor of Nanoelectronics at the Department of Electronic and Electrical Engineering, University College London

Dr Max Migliorato is Senior Lecturer at the School of Electrical and Electronic Engineering, the University of Manchester

Dr Jon Willmot, is Lecturer at the Department of Electronic and Electrical Engineering, the University of Sheffield

Dr Rick Smith, is Lecturer at the Department of Electronic and Electrical Engineering, the University of Sheffield

Dr Qiang Li is Lecturer at the School of Physics and Astronomy, Cardiff University

Dr Siming Chen is a Royal Academy of Engineering Fellow and a Lecturer in the Department of Electronic & Electrical Engineering at UCL

Key associated and research staff

Dr Angela Sobiersierski
Dr Chris North
Dr Harry Gordon-Moys
Dr James Sexton
Dr Jae-Seong Park
Josie Nabialek
Dr Majid Salhi
Dr Mingchu Tang
Dr Roberto Quaglia
Dr Saleem Shabbir
Steven Akin
Dr Sheng Jiang
Dr Richard Forrest
Wendy Sadler MBE
Dr Wyn Meredith
Dr Yuefei Cai
Dr James Watson
Dr Saad Muttlaak
Dr Nicolas Poyiatzis

PhD students

Ahmed Alquradhi
Alex Lindley
Andrew Hadfield
Ben Maglio
Curtis Hentschel
Dominic Kwan
Guillem Martinez De Arriba
Fwoziah Albeladi
Hui Jia
H.Deng
Jack Baker
Jack Haggar
Joe Mahoney
Junjie Yang
Lydia Jarvis
Maryam Alsayyadi
Manyu Dang
Nourh Almalki
Peng Feng
Reem Alharbi
Ruslan Murshudov
Shuoheng Shen
Tahani Albiladi
Wei Zhong

Administrative Staff

James Atkinson
Kate James
Katherine Greenacre
Grace Mullally