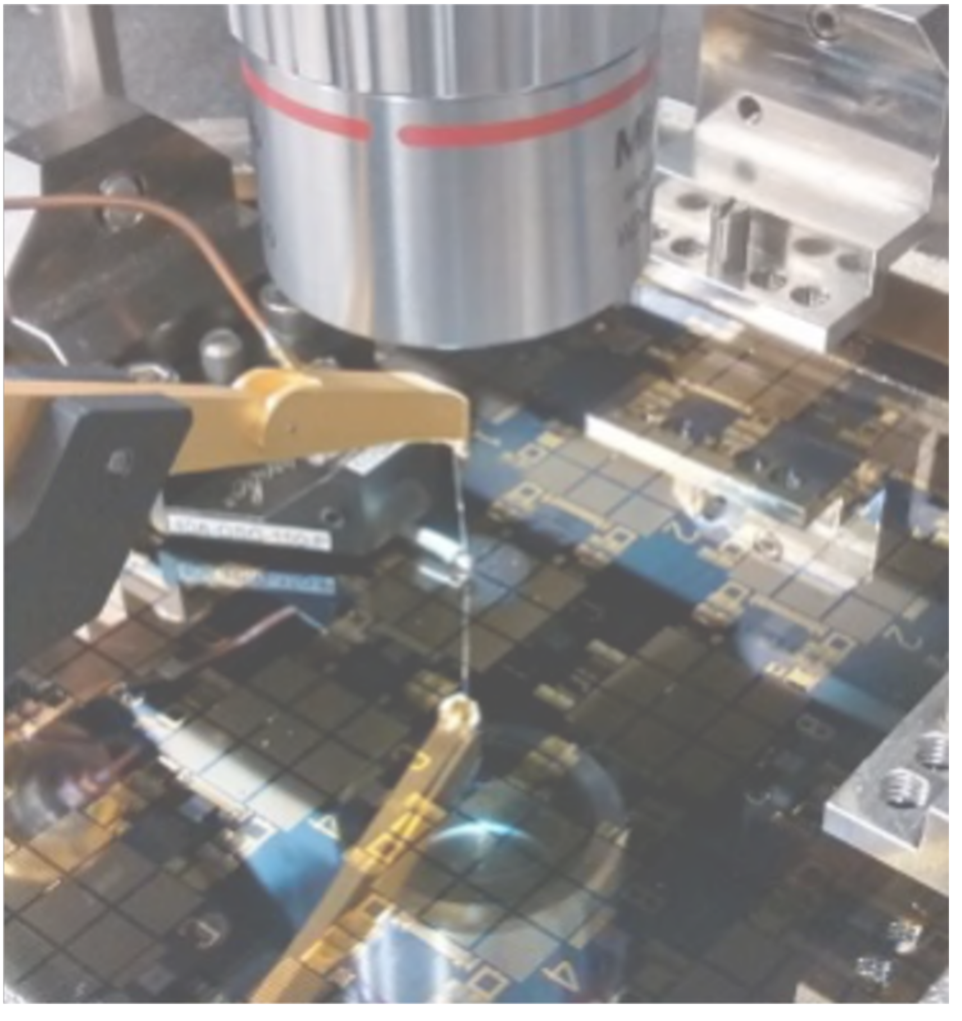
Future Compound Semiconductor Manufacturing Hub

Annual Report 2022



Establishing the UK as the primary global CS research and manufacturing hub

Grant number
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Engineering and Physical Sciences Research Council

https://compoundsemiconductorhub.org

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WELCOME MESSAGE

Prof Peter Smowton, CS Hub Director

Welcome to the Annual Report of the EPSRC Future Compound Semiconductor Manufacturing Hub. This year has been one of tremendous progress and opportunity with some remaining difficulties due to damaged supply chains. The CS Hub has played a full part in building the future for Compound Semiconductors (CS) in the UK and contributing to investigations into, and planning the future strategy of, semiconductor manufacturing by four different parts of UK government; these include the Department of Business, Energy and Industrial Strategy, the Department of Digital, Culture, Media and Sport, the Foreign, Commonwealth and Development Office and the Government Office for Science. We have also contributed to other sector led initiatives such as by the Institute of Physics evaluation of the role of Physics in UK Manufacturing. We have made significant scientific advances and extended capability as will be described elsewhere in this annual report. Most pleasingly we have seen the development of all of our staff with new skills and responsibilities, with this being reflected in the promotion and development of many individuals to more independent and to academic positions.

The Hub started as a partnership between Cardiff University, the University of Manchester, the University of Sheffield, University College London and 24 original industrial backers. Through feasibility and follow on funding we have added contributors from the Universities of Bath, Bristol, Cambridge, Lancaster, Oxford, Strathclyde, Swansea and Warwick and now actively engage with over 30 industrial partners and other organisations including other Manufacturing Hubs and centres of critical mass such as the EPSRC National Epitaxy Facility.

As a response to COVID in the last year we made a number of videos explaining the role of the Hub and how new partners could interact with us and for use in the training of staff, even when close contact was difficult. Some of these can be seen on our website About Us – The Future Compound Semiconductor Manufacturing Hub (compoundsemiconductorhub.org) . We also received a number of high profile visitors and some of these visits are described in the Outreach section below.

One of the key ambitions of the Hub was to do the science that enabled the scale-up of manufacturing of CS components and in this context I am delighted to see the announcement this year by one of our partner companies IQE. Following the development of fabrication technologies and methods for characterisation including the rapid turnaround, so called "fast fab" characterisation by the CS Hub, IQE have announced the world's first commercially available 200mm GaAs based VCSEL wafers IQE announces the world's first commercially available 200 mm (8") VCSEL wafer | IQE Corporate (iqep.com). The underpinning science base developed by the Hub together with world leading expertise in crystal growth at IQE has enabled UK leadership in manufacturing in this important technology area. Going forward scale-up will remain an important focus for the CS Hub with further significant scientific and technological developments required to enable large scale manufacturing of other device types.

Finally I was delighted to start back at in-person conferences, such as Photonics West, with the opportunity to exchange ideas and results with colleagues from academia and industry. The CS Hub run SIOE conference this year was also in-person and maintained the record attendance figures seen at the previous on-line event. The extremely vibrant conference was held over 3 days and featured the new 400 seat, state of the art lecture theatre in the Centre for Student Life at Cardiff University. Industry sponsorship included that from Hub partners Photon Design, Huawei, Institute for Compound Semiconductors and the Compound Semiconductor Centre Ltd and supported the event and enabled a number of the best student presenters to leave with recognition for their excellent work. The CS Hub looks forward to another full and exciting year.

INTRODUCTION

EPSRCs vision for their critical mass investments is to support UK manufacturing industries by supporting the commercialisation of early stage research opportunities in emerging areas, through a network of Future Manufacturing Research Hubs.

Each Hub has a programme of innovative research in the engineering and physical sciences, related to the challenges in commercialising early stage research. A key characteristic of the Hub model is that the research is driven by the long-term research challenges of users. User collaboration is therefore an essential aspect for these Hubs.

The vision of The Future Compound Semiconductor Manufacturing Hub (CS Hub) is to establish the UK as the primary global research and manufacturing hub for Compound Semiconductor (CS) Technologies by combining and connecting the UK research excellence in CS, with the very best translational facilities and the new Compound Semiconductor Catapult to support the UK CS industry and UK industry users of CS. The combined activity provides a path from enabling fundamental research through wafer, device and integrated chip manufacturing research into prototyping, reliability testing and system qualification.

The CS Hub has 3 key outcomes:

- To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
- To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
- To generate novel integrated functionality such as sensing, data processing and communication.

The Hub forms an integral part of the CS Cluster based in South Wales, and also serves and supports CS manufacturing and applications related industry throughout the UK. The CS Cluster forms a complete manufacturing chain from Technology Research Level (TRL) 1 to 9 and currently comprises 9 collaborating partners. The Hub makes use of the world leading facilities and expertise at the Institute for Compound Semiconductors (ICS, Cardiff University) and feeds the higher TRL 4+ activity at the Compound Semiconductor Centre (CSC) which links to the UK manufacturing industry and the Compound Semiconductor Catapult. The Hub is resourced to research and develop new manufacturing processes, leveraging existing capital investment and completing the Welsh and UK Government strategy to generate a major UK CS Cluster.

Compound semiconductors are essential for the development of:

- 5G
- energy efficient lighting
- smart devices
- electric vehicles
- imaging techniques

Compound semiconductors are vital to development of technologies supporting:

- a connected world
- health
- security
- the environment.

The Hub will:

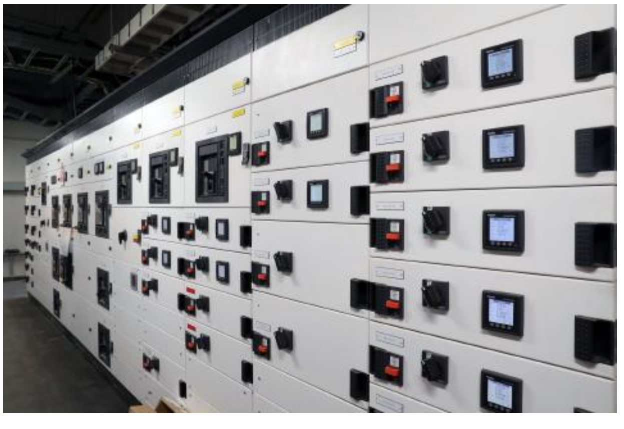
- position the UK at the centre of CS manufacturing research
- support & promote CS research and systems research in all associated fields
- apply the manufacturing disciplines and approaches used with Silicon semiconductors
- combine CS with Silicon to generate the required increase in CS manufacture.

INTRODUCTION

Translational Research Hub

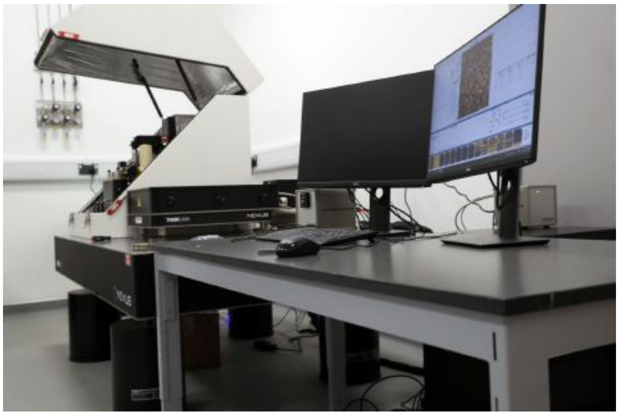
The Translational Research Hub (TRH) at Cardiff University is due for completion in the coming months. Designed by HOK London Studio, the 129,000-sq-ft. research hub will be home to two scientific research establishments – the Institute for Compound Semiconductors and Cardiff Catalysis Institute.

The building boasts laboratories, offices, bespoke clean rooms and microscopy suite. These spaces will be available to business partners, who will work with TRH's academic experts to develop industrial solutions.



High-tech lab space will support excellent research alongside facilities designed for industrial collaboration, helping to overcome traditional barriers between academia and commercial application.

Translational Research Hub



The building is designed to inspire the imagination, foster the health and wellbeing of building occupants and serves as a showcase space for attracting and retaining top-tier students and researchers.

A central atrium serves as an event space where visitors can peer into labs to see the ground-breaking research underway

HUB STRUCTURE

Our Hub of CS research activity and operational headquarters is located at Cardiff University, led by Hub Director, Professor Peter Smowton. This central entity interacts highly with spoke including universities: University of Manchester, University of Sheffield and University College London, as well as a large number of industrial partners and collaborators.

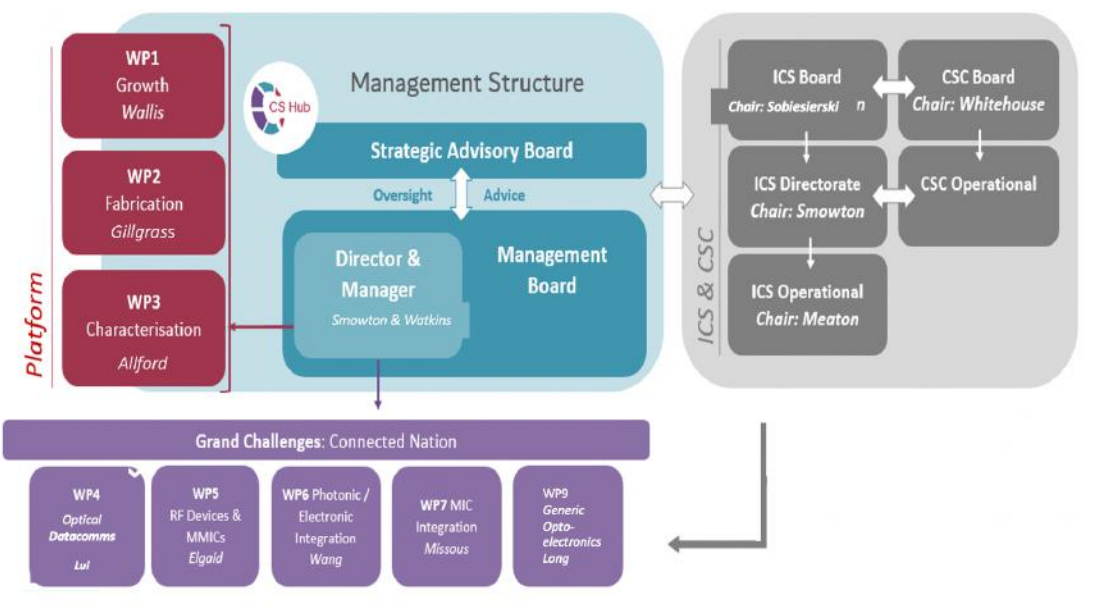
The Hub structure includes a Management Board and Strategic Advisory Board, as well as support structures for each of the Hub's 8 work packages.

Management Board

The Hub Management Board (MB) is responsible for the strategic and operational management of the Hub, including making decisions on the allocation of funding. The MB is comprised of a number of senior Hub members who are able to represent the research interests of the Hub. All members meet quarterly to discuss and plan the research of the CS Hub, in addition to other areas the MB is responsible for, including ED&I and learning and development. The MB reports to the Hub Strategic Advisory Board (SAB) every 6 months.

Strategic Advisory Board

The SAB provide guidance to the Hub MB via a biannual meeting. The Board includes world leading research and industry experts in the field of compound semiconductors. Strategic Advisory Board meetings provide an opportunity for Hub members to receive guidance and direction from impartial, highly experienced and knowledgeable individuals.



The CS Hub Management Structure. The Director is advised by a Management and Strategic Advisory Board.

HUB STRUCTURE

CS Hub Management Board members

Prof Huiyun Liu	University College London
Dr. Wyn Meredith	Compound Semiconductor Centre
Prof. Mo Missous	University of Manchester
Prof. Peter Smowton	Cardiff University
Prof. Paul Tasker	Cardiff University
Prof. Tao Wang	University of Sheffield

Strategic Advisory Board members

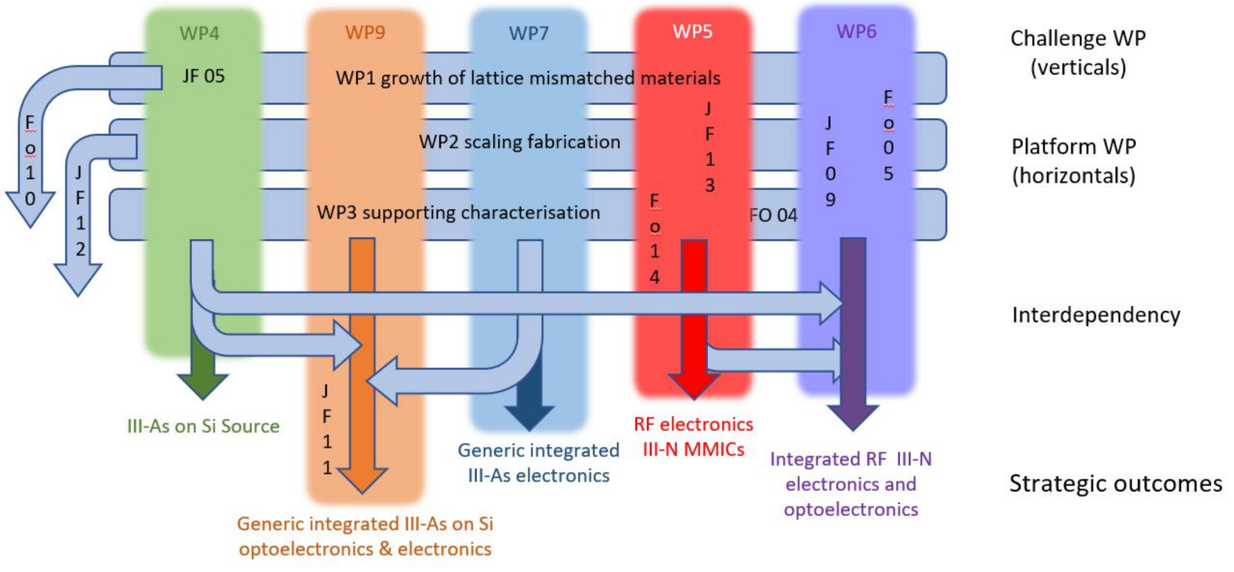
Dr. John Bagshaw	Independent Technology Consultant
Dr. Maria Ana Cataluna	Heriot-Watt university
Dr. Ivona Mitrovic	University of Liverpool
Prof. Richard Penty	Cambridge University
Prof. Dominique Schreurs	KU Leuven
Dr. Andy Sellars	CSA Catapult
Dr. Carol Trager-Cowan	University of Strathclyde

Hub Work Package Leads

Prof. David Wallis	Cardiff University	WP1 Lead
Dr. Sara-Jayne Gillgrass	Cardiff University	WP2 Lead
Dr. Craig Allford	Cardiff University	WP3 Lead
Prof. Huiyun Liu	University College London	WP4 Lead
Prof. Khaled Elgaid	Cardiff University	WP5 Lead
Prof. Tao Wang	University of Sheffield	WP6 Lead
Prof. Mo Missous	University of Manchester	WP7 Lead
Dr. Yun Long	Cardiff University	WP9 Lead

Membership of the CS Hub management structures is shown in the tables above. The Hub is governed by a Management Board made up of senior members of the Hub team across the four original academic partner institutions.

The Strategic Advisory Board is made up of experts from academia and industry who are well equipped to advise the Hub on research direction, identifying commercially valuable research and advising on impact paths. Our work package and grand challenge leads direct and coordinate the research of the Hub.



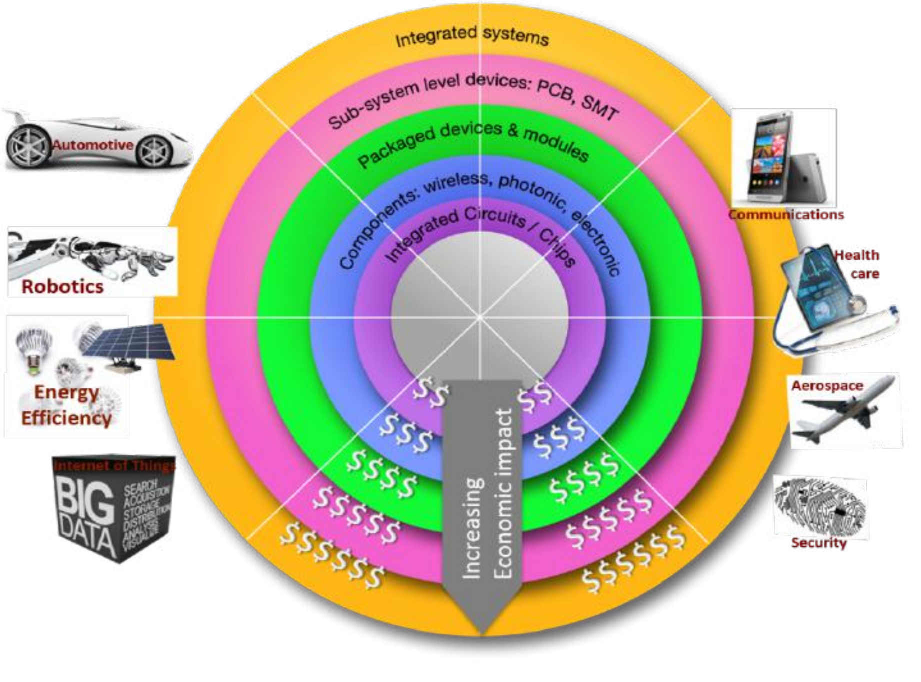
Work Package (WP) structure of the CS Hub. Grand challenge WPs are supported by 3 "platform" areas and have been made more effective by the addition of a number of feasibility (JF) and follow-on (FO) activities from other universities, together focussed on achieving the strategic outcomes.

Next generation technologies will only be achieved with a huge increase in compound semiconductor manufacture.

Compound semiconductor materials are a Key Enabling Technology at the heart of modern society.

Key Outcomes:

- To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
- To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
- To generate novel integrated functionality such as sensing, data processing and communication.

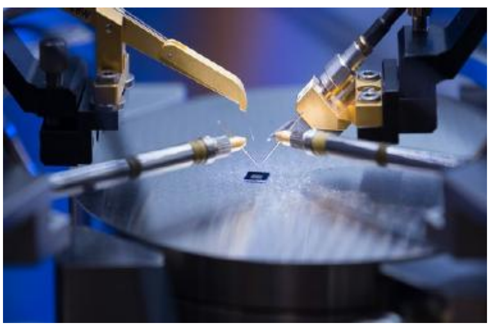


The diagram indicates the likely impact areas of technology developed via the CS Hub and emphasises the added value at each stage enabled by the CS technology.

CS Cluster developments

The Hub remains an active and founding member of the CS Cluster in South Wales. CSconnected is the formal gateway to the Cluster which represents organisations directly associated with research, development, innovation and manufacturing of compound semiconductor related technologies, as well as organisations along the supply chains whose products and services are enabled by compound semiconductors.

Other members of CSconnected include core partners, the Institute for Compound Semiconductors (ICS, Cardiff University), the Compound Semiconductor Centre Ltd (CSC), the Compound Semiconductor Applications Catapult and the Centre for Integrative Semiconductor Materials (CISM, Swansea University). These are joined by business partners IQE plc, SPTS, Microchip, and Nexperia Newport. Together we complete the supply chain for bringing new CS discoveries to market. The development of the CSconnected brings us closer to achieving our mission of "establishing the UK as the primary global CS research and manufacturing hub"



CCR City Deal

Significant investment (£37.9m) from the Cardiff Capital Region (CCR) City Deal has enabled Cluster members, IQE plc to develop a new high-tech facility in Newport. This has generated employment for a number of highly skilled engineers and technicians.

Image adapted from CS Catapult material. The CS Hub covers TRL levels 1 to 4 and works together with ICS, the CS Centre and the CS Catapult, together with several other partners, to form the CS Cluster.

Societal

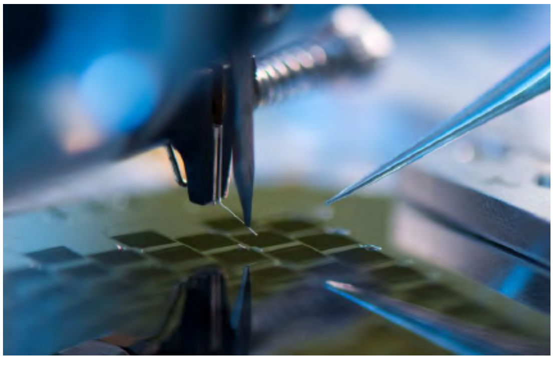
Compound Semiconductor materials are a Key Enabling Technology underpinning the operation of the internet and enabling emerging megatrends such as smart phone usage, satellite communications/GPS, direct broadcast TV, energy efficient lighting, efficient solar power generation, advanced healthcare and ground breaking biotechnology. Simply put these technologies support our connected world and the future health of the planet.

Knowledge Dissemination

We are active in dissemination of knowledge via conferences such as UK Semiconductors and Photonics West, the latter providing an excellent mix of science and commercial activity. We publish in open access peer reviewed journals such as those from both the Nature and IEEE stables. Our aim remains to engage new partners and we hold workshops, use feasibility funding, actively canvas and make use of our existing partners and contacts, relevant KTNs and other appropriate bodies to connect as widely as possible.

Outreach

We have recently recruited a new outreach officer, Chermaine Barrett and will be progressing more in-person outreach next year. More information is provided in the outreach section from page 36.



Skills Base

The cutting edge equipment operated as part of a manufacturing process offers an excellent training opportunity, inculcating a manufacturing mind set in a UK strategically relevant high technology field. We embed technological excellence and the latest manufacturing approaches in UK industry. PDRAs and students participate in high level meetings with the commercial organisations and work alongside R&D staff from industry. There is also a direct economic impact via the provision of skilled workers to relevant companies.

Economic

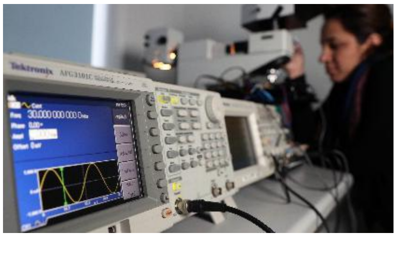
Our vision is to ensure that the UK's research strength in compound semiconductors will be embedded in manufacturable approaches so the UK can commercially address the opportunities that compound semiconductors will provide. The global market for compound is expected to grow to 44.5 billion USD by 2027. Expanding commercial activity in the compound semiconductor sector will provide an important boost for the UK economy and maintain UK advanced manufacturing competitiveness. A good example of this is Cardiff headquartered IQE Plc, the global leader in supplying compound semiconductor materials (with turnover of 178m, 2020 results).

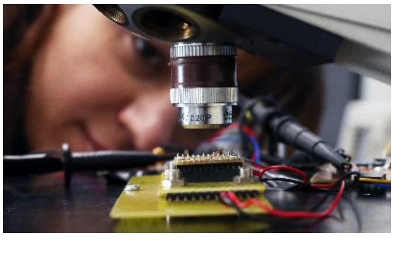
Our aim is to strengthen the relationship between academia and industry and this will be achieved by 1) changing the mind set of researchers to start from solutions that allow rapid translation to production by providing access to production scale and research tools that are functionally similar along with highly skilled support for the tools and processes; 2) Co-location of research and industry staff to maximise cross fertilisation of ideas, techniques and approach in an environment that supports interaction. The Hub together with staff from the Compound Semiconductor Centre will support SMEs through product prototyping, IP generation, skills development and training. They will help bid for external grants, coordinate partner forums, form networks and prepare roadmaps.

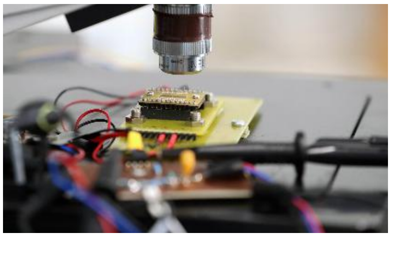
As early as 2014 the Sheffield led EPSRC III-V centre CS roadmap identified a concern that the UK CS community was missing an exploitation link to help provide a route to impact and exploitation. Many technological solutions work well in the research environment but fail to succeed commercially. The Hub directly addresses this issue, by working to change the academic community mind set, to inspire researchers, via training and environmental changes, so they begin with solutions that allow rapid translation.

The Hub is encouraging the co-location of research and industry staff to maximise interactions. Our research is specifically designed to produce intermediate outputs that can be used to demonstrate the potential for successful translation. In order to promote this activity across the wider UK community, the Hub had £1m to invest in new research projects (described in more detail in the feasibility study section of this report). We invested in a first round of 6 initial short-term projects, followed by 4 continuation studies and 5 new studies as a result of our joint feasibility 2019 call with other manufacturing hubs. Funded studies have a high probability of translatable manufacturable research, and are expected to cascade into subsequent larger studies with an emphasis on translating technology from research to industry. We recognise that SME engagement is a critical element in promoting rapid exploitation opportunities and interact with a number of these.

Future Compound Semiconductor Manufacturing Hub	Institute for Compound Semiconductors	Compound Semiconductor Centre	Compound Semiconductor Applications Catapult
CS Manufacturing Research	Facilities; Equipment; Services (skilled workers)	Develop and prototype CS materials	Accelerate the development of products using compound semiconductors
Enable high value & productivity in CS manufacturing	Scale Fabrication	Enable a wide range of applications	Market intelligence Consortia building Supply chain management Project management
Building on CS research	Product development to prototyping	Translate R&D to product & process innovation to high value large scale manufacturing	Design studio with simulation and modelling Power electronics lab Photonics lab RF/microwave lab Advanced packaging lab
Training; Outreach	Industrial collaboration		Knowledge Transfer Partnerships







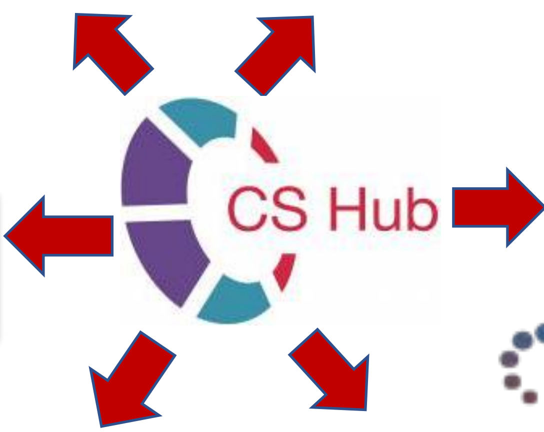
Images show device development by a Hub PhD student, Cardiff University.

Translational funding

The Hub strives to connect its EPSRC research activity through e.g. Innovate UK funding to higher TRLs and commercial exploitation. As planned further translational funding with industry partners is driving this impact route. Since the start of the Hub several translational Innovate UK projects have begun, and industry partners have provided funding for studentships via either CASE awards or via cofunding with the EPSRC Centre for Doctoral Training in Compound Semiconductor Manufacturing. Technology developed in the Hub is also embedded in the Institute for Compound Semiconductors and the EPSRC National Epitaxy Facility, which are both open access facilities for UK academics and UK industry.

MAG-V : Enabling Volume Quantum Magnetometer Applications through Component Optimisation & System Miniaturisation. Innovate UK

Quantum Electro-Optic Detector Technology(QuEOD). Innovate UK



Strength in Places. CSconnected UKRI

SLOGaN M4 – Short Loop Optimisation of Gallium Nitride Materials and Major Manufacturing Modules. Innovate UK

Kairos. Innovate UK

EXPLOITATION ROUTES DRIVING IMPACT

Qfoundry. Innovate UK

GaN on SiC RF. Smart Expertise

CS Hub

Studentships CASE, for example with:

Research and skills surveys

In order to understand the areas of Compound Semiconductor research of most interest to our industry partners and their skills challenges and needs, the Hub developed research and skills surveys. We shared the surveys with a range of new and existing industry partners to gather the best insights in these areas.

The insights gained helped us as part of a wider review of the Hub's research and supported our future planning. The surveys also helped us to understand the specific challenges industrial partners have faced as a result of Covid. The Hub Management Board and Strategic Advisory Board have used the surveys insights to further inform discussion on the Hub's strategic direction and the responses have also provided the basis for a series of more in-depth discussions with industry partners.

Packaging the future – connecting semiconductors to the consumer

The CS Hub and CSA Catapult recently hosted (May 2021) an interactive online workshop, exploring the challenges and added value of advanced (packaging) semiconductor integration. The aim of the event was to get packaging considered and included at an earlier stage during the device development phase, with researchers and industry partners discussing key challenges and solutions. The workshop was attended by over 30 academics and industry partners, with four presentations from the Hub on mature projects looking for routes to commercialisation and earlier stage issues around integrated circuits. Four industry partners subsequently presented on their capabilities, and this was followed by an engaging roundtable discussion with a wider set of academics and industry partners. The event provided a forum to discuss long established challenges and will foster further collaboration between the Hub and industry. Below are some quotes from industry partners who attended and presented at the event:

"It was an excellent opportunity to expose the breadth of packaging challenges and evolving solutions that need to be catalysed in UK".
Geoff Haynes: Business Development Manager at RAM Innovations Ltd.

"A really useful workshop highlighting the importance of, and a rallying call, to take packaging seriously from the start".
Glenn George: Managing Director at Bay Photonics ltd

"I thought the event was well organised and gave an interesting insight into the research being done, and how that can blend with the innovations in the UK packaging industry".
Matt Booker: Head of Sales – Assembly Services at ALTER TECHNOLOGY TÜV NORD UK Ltd

"I found it very informative to learn about technologies outside my immediate field, discuss the packaging challenges we all face and understand how our collective capabilities could address those".
Ross Wheeler | III-V IR Product Development Manager & Technical Authority | Space Imaging

Photon Design develops software for the design and simulation of semiconductor optoelectronic components. Based in Oxford we now market our software tools in over 30 countries across the globe. The EPSRC Future Compound Semiconductor Manufacturing Hub (CS Hub) is now very active in developing the manufacturing of such components, providing true state-of-the-art capabilities in the UK. The field of optoelectronics is a key growing technology – including the expected integration of optoelectronics for even short range datacom. The CS Hub is providing valuable support to maintain the strength of optoelectronics in the UK. It is very valuable for us to be involved in such activities and has already contributed data on the performance of VCSEL devices, helping us develop our advanced Harold VCSEL simulation tool, and will soon give us access to valuable measurement data on integrated photonic structures to feed back to our models.
Dominic Gallagher: CEO, Photon Design

IQE plc, headquartered in Cardiff, manufactures compound semiconductor epitaxial wafers, using both MOCVD and MBE technologies from its sites in Europe, North America and Asia. It has pioneered the supply of custom-designed wafers for a number of vertical device technologies for over 30 years, utilising an open-access and pure-play business model. Its global business has been dependent on supplying wafers used in a broad range of electronic and photonic epitaxial device structures and serving end-use market applications in wireless and optical telecommunications, medical, industrial and consumer markets amongst others.
Partnering with the epitaxial structure design, modelling and the developing device fabrication capabilities at the The EPSRC Future Compound Semiconductor Manufacturing Hub (CS Hub) has enabled IQE to characterise and test its material for the development of new epitaxial technologies and also for quality assuring product for its customers. The capability within the CS Hub allows for development towards industry- relevant wafer processing at the emerging ICS centre, enabling an acceleration within the innovation landscape towards pre-commercialisation of photonics GaAs and InP products and for RF and Power GaN-based devices.
Iwan Davies, IQE plc Group Technology Director

EPSRC CENTRE FOR DOCTORAL TRAINING (CDT)

Overview

Our partner activity, the EPSRC Centre for Doctoral Training (CDT) in Compound Semiconductor Manufacturing is now in its third year. The CDT currently has 32 students in Cohorts 1 to 3, with a further tranche of up to 14 students joining us in October 2022. A total of 65 students are expected over the five intakes of the current EPSRC funding. Our aims are to:

- Develop PhD graduates with multidisciplinary skills in a highly research active area, including training and experience in a clean room environment.
- change the face of CS research in the UK by training the new generation to understand how to facilitate the translation of research into production
- Support UK companies by exploiting the highly advantageous electronic, magnetic, optical and power handling properties of CS and pioneering novel integrated functionality
- drive new linkages within the UK industrial supply chain including with CS sub-systems users to facilitate innovation in their product offering.

The CDT has a structured training programme in the first year, based on the MSc in Compound Semiconductor Physics or Electronics, delivered by Cardiff University which includes practical cleanroom training. Alongside the MSc modules, the cohort participate in research seminars offered by our partner universities, University of Manchester, University of Sheffield and UCL to broaden their understanding of key issues in CS research.

In the spring semester, we run skills sessions in topics such as Intellectual Property and Commercialisation, Responsible Research and Innovation, and Equality Diversity and Inclusion, as well as the 'Manufacturing Methods' seminars offered by our industrial partners, exposing students to topics in the manufacturing chain. During 2021-22, the topics were:

- Market and Industrial manufacture of III-V Semiconductor lasers: Ning Zhang, CSA Catapult
- Development of III-V Based IR FPA Detectors and Associated Manufacturing Capability: Ross Wheeler, Teledyne E2V
- Practical Project Management: Ali Anjomshoaa, Compound Semiconductor Centre
- Business Alchemy: Turing Ideas into Cash: Frazer Anderson, Oxford Instruments
- An Overview Of High Volume Semiconductor Device Manufacturing: James Nugent, Huawei
- From Net Waste to Net Zero: Sam Evans, Nexperia
- Site Visit: Nexperia

Students have welcomed the return to face-to face teaching and activities and have taken part in both the SIOE conference and the UK Semi Conferences this year. In November 2021 Cohort 2 organised a superb event showcasing the work of Cohort 1 and with keynoter speakers from Huawei and IQE. We look forward to inviting supervisors and industry contacts to a similar student-led event this November.

We have continued to have strong involvement from our industry partners, especially for the co-funding of PhD projects. In Cohort 1, five out of six projects have industrial co-funding, in Cohort 2 it's 10 out of 13, while 11 of the 13 students in Cohort 3 have co-funding from an industrial partner. We are grateful for the support of:

- Compound Semiconductor Applications Catapult
- Compound Semiconductor Centre
- Alter Technology
- Huawei
- IQE
- Leonardo MW
- Linwave
- Mitsubishi
- National Physical Laboratory
- Nexperia.
- Oxford Instruments
- Qorvo
- The Rockley Group
- SPTS Technologies
- Photon Design
- Applied Nanolayers
- Teraview
- Zeiss

Cohort 3 Students at their induction day

We are actively seeking additional partnerships through conversations with companies about their research and development needs. Please contact the CDT at semiconductors-cdt@cardiff.ac.uk if you have an idea for a research project and need to find an academic contact in a relevant area to help you develop a project proposal for a CDT student. Alternatively we can match you with current projects to help refine them to your interests. . Industry partner funding of £12.67k is required for each of the three PhD years to part-fund a student within an amazing
academic network in the wider semiconductor community.
Other options for involvement in the CDT include industrial placements, guest lectures and careers fairs.

The CS Hub investigators and associated groups have been carefully selected for their track record in innovation and impact, complementary technical capability and the individual skill sets that can combine to create new solutions to the identified major scientific challenges in manufacturing. Expertise in epitaxial growth, including growth on non-native substrates is provided by Li, Liu, Missous, Wallis, and Wang. Buckle, Elgaid and Missous bring experience of wafer scale-up and manufacturing uniformity over these larger wafer sizes. Abadia, Beggs, Quaglia, Smowton and Tasker bring world leading expertise in design, integration and characterisation.

Leading Academics

In addition to the Hub's Work Package Leads, we work with a number of world-leading academics to develop the highest impact research possible under the remit of the Hub. Michael Pepper FRS, FREng (UCL) (h-index 55, 8 patents) is Pender Professor of Nanoelectronics and has received the Royal Society's Bakerian Prize Lectureship, Hughes and Royal Medals. He is co-founder and Scientific Director of THz technology spin-off company TeraView. He is a former member of General Board and Council of Cambridge University and Council for Industry and Higher Education.

Alwyn Seeds FREng, FIEEE (UCL) is Professor of Optoelectronics. He pioneered the research area of microwave photonics and was awarded the Gabor Medal and Prize of the Institute of Physics in 2012. He is an inventor on 16 patents and is co-founder of Zinwave Ltd, which is now the third largest supplier of wireless over fibre systems in the world and was acquired by McWane Technologies Inc. in 2014.

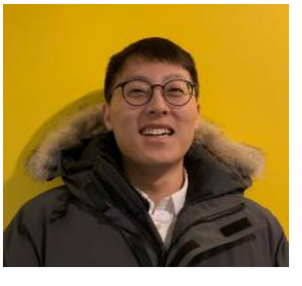
These staff are supported by academics Rick Smith & EPSRC Manufacturing Fellow Jon Willmott (Sheffield), Max Migliorato (Manchester), and Senior Research Fellows Siming Chen, Minchu Tang (UCL) and Sang Soon Oh (Cardiff) covering design, nitride fabrication, and characterisation and growth of CS on Si.

Flexibility

The Hub has worked flexibly to ensure that our research remains highly relevant in the constantly evolving CS manufacturing environment. We have welcomed several new people to the team, bringing with them a variety of expertise essential to keep the Hub at the very peak of research excellence. Dr Yun Long has taken over leadership of Work Package 9 (Generic Photonic Integration) from Nicolas Abadia. Dr Yun bring expertise is in semiconductor optoelectronics, with a background in materials characterization

New expertise

The Cardiff lab team have also been joined by a new post-doctoral research associate: Dr Pawan Mishra, Dr Zhongming Cao and Dr Chris Woodhead. Dr Mishra (h-index 11) has a strong background in Compound semiconductor-based Optoelectronics devices. Presently Dr Mishra research focuses on developing selective area intermixing processes and implementing efficient Photonics Integrated Circuits without resorting to the regrowth methods.



Dr Cao recived his PhD degree in Electrical Engineering and Electronics from the University of Liverpool. Prior to the Cardiff University, Dr Cao was research associate at Lancaster University, working on MBE growth of type II quantum materials for gas sensors. Dr Cao research interest includes III-V compound semiconductor materials, dilute nitrogen and bismuth alloys, antimony-based alloys for photodetectors, mid-infrared sensing, and optoelectronic application

Dr Chenqi Zhu has joined the University of Sheffield as a post-doctoral research associate.

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WORK PACKAGE 1

Materials Growth (Epitaxy)

Summary: Work package 1 brings together all the compound semiconductor growth activities being undertaken with in the Future Compound Semiconductor Manufacturing Hub. This covers a diverse range of materials systems, including Nitrides, Arsenides and Phosphides. A key focus of this work is the growth of device structures on to substrates that are compatible with, low cost, large volume manufacturing to allow exploitation of the technologies developed in commercial markets.

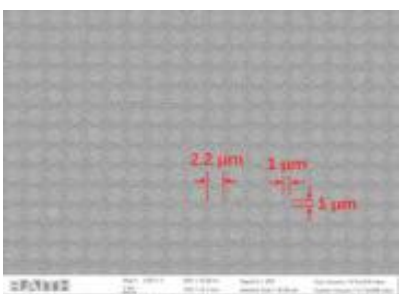
Lead : Prof. David Wallis Email: WallisD1@Cardiff.ac.uk

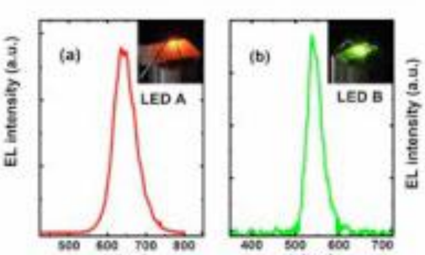
Contributing academics: Tao Wang (Sheffield), Mo Missous (Manchester), Huiyun Liu (UCL), and Qiang Li (Cardiff). We also have 2 project partners, Prof. Manus Haynes (Lancaster) and Dr Philip Shields (Bath), who are working on a Future CS Hub sponsored feasibility studies. .

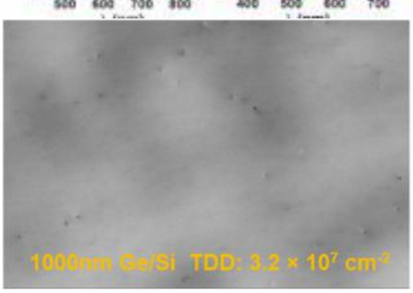
WP1 encompasses all the epitaxy activities that are relevant to the CS Hub. By bringing together the research activities at different universities it allow experience and best practice to be shared across the groups to solve problems and extend individual capabilities.

Progress and challenges: Over the last year COVID restrictions have been slowly lifted across the Hub partner universities. This has allowed researchers to get back into their laboratories and rekindle their development activities. These activities have included completing the commissioning of some new equipment which was started back in 2021 but had been delayed by the unavailability of installation engineers due to international travel restrictions. Specifically, at UCL commissioning of a new Veeco MBE system will significantly decrease impurity backgrounds in Arsenide and Phosphide based layers and also allow scale up to 76mm wafers. At Sheffield and Cardiff, upgrades to in-situ monitoring hardware on the MOCVD growth systems will improve the ability to measure parameters such as temperature, roughness and wafer bow in real time improving control of the growth processes being developed.

In addition to the upgrades to growth hardware, there have also been some exciting developments in the materials technologies under development:







Prof. Tao Wang at Sheffield has been developing a novel approach to overcome the performance limitations of microLEDs for several years now. For standard LEDs, devices are usually defined by etching structures into the LED layers, however, this results in a significant fall off in performance as the devices are reduced below about 10um. Prof. Wang's approach involves the regrowth of micron sized devices on to patterned substrates, avoiding the etch damaged cause by the conventional approach. Over the last year Prof. Wang has demonstrated the ability to produce 2micron diameter regrown LEDs which can emit both green and red light on the same growth run on different templates using a multiple wafer MOCVD system . This is important for full colour microLED displays which require red, green and blue emitters.

Prof. Liu's lab at UCL has been developing new approaches to allow quantum-dot lasers to be produced on Silicon substrates. To this end, Molecular beam epitaxy (MBE) has been used to deposit Germanium buffer layers which have a close lattice match to GaAs on Silicon substrates. Work optimising a whole range of parameters including, growth temperature and temperature ramping between different parts of the structure, use of Antimony Surfactants, buffer layer thickness, Sb and Si co-doping and post growth annealing have delivered layers with <4x1017 cm-2 threading dislocations. This is an important step to allow quantum dot laser to be manufactured on a Si platform.

Scaling Fabrication

Summary: This work package is addressing the key challenge of fabricating high quality and reproduceable compound semiconductor devices over large format wafers. Due to the relative ease of on-wafer characterisation the fabrication of structures such as VCSELs and passive components on GaAs substrates is providing a test bed for developments which are being applied to allow, low cost, large volume manufacturing of the devices being developed in other work packages in the Manufacturing Hub.

Lead : Dr Sara-Jayne Gillgrass Email: gillgrasss@cardiff.ac.uk

Contributing academics: Prof. K. Elgaid, Dr Q. Li, Prof. M. Missous & Prof. P. Smowton.

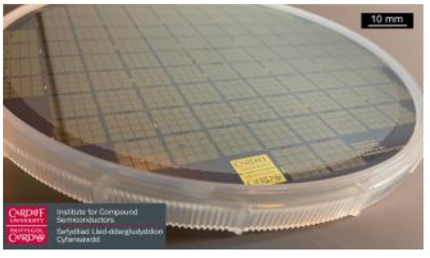


Figure 1: *150 mm wafer containing 154,000 individual VCSEL devices*

In work package 2, we are dedicated to developing reliable and reproducible fabrication processes, particularly across large format wafers (>100 mm). Working alongside colleagues at Cardiff University's Institute for Compound Semiconductors (ICS) allows cross fertilisation of ideas and a route to impact and knowledge transfer of CS Hub innovation using the cutting-edge ICS fabrication facilities for wafer diameters (currently) up to 150 mm. Here we profile an example of the issues arising and the required solutions in the manufacture of VCSELs over large wafer areas

Progress and challenges: High-volume consumer applications of VCSEL arrays have proliferated in recent years forcing the semiconductor manufacturing industry to transition from 100 to 150 mm substrate sizes to cope with the expanding market, with an increasing requirement even beyond 150 mm. Growth of e.g. VCSEL structures over these wafer diameters, on GaAs, is nontrivial, with large amounts of compressive strain resulting in wafer bow/warp. The use of Ge substrates is one potential route to mitigate this with additional benefits, such as increased mechanical stability.

Our established 150 mm VCSEL fabrication process has been used to investigate manufacturing and performance variation of nominally identical epitaxial structures. Figure 2 shows the difference between wafer bow of these structures grown on Ge and GaAs, with a 5x magnitude difference at x=0.

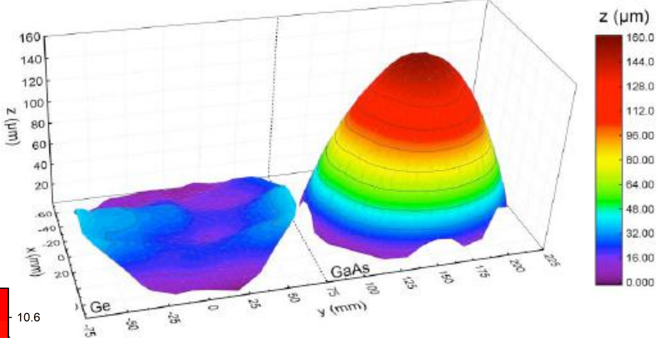


Figure 2: *Wafer bow measurements of VCSEL structures over 150 mm Ge (L) and GaAs (R) .*

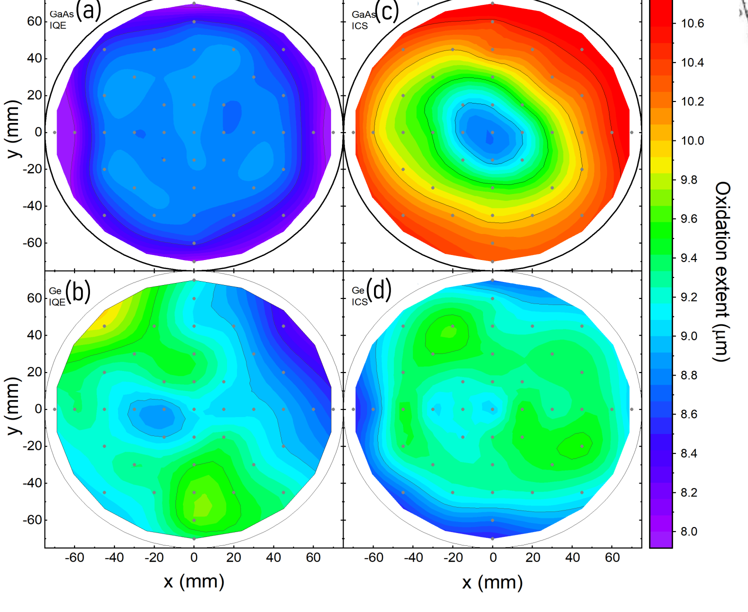


Figure 3: *2D contour plots of oxidation variation across Ge and GaAs wafers, in a tube furnace (a) & (b), and single-wafer furnace (c) & (d).*

Non-uniform heating during one of the oxidation steps in VCSEL manufacture, caused by the wafer bow and non-uniform contact, creates a large oxidation extent variation, as in figure 3(c), due to the exponential dependency of oxidation on temperature. This hides real epi-layer non-uniformity and device performance in large area wafers. In comparison, GaAs oxidised in a tube furnace (figure 3a), heated by ambient temperature, exhibits only the small variation due to changes in epitaxy.

Ge on the other hand, exhibits no radial performance variations regardless of oxidation method chosen. Here, device non-uniformity is driven by oxidation once again, but is due to epi-layer variations.

Fast Fab and Characterisation

Summary: This work package is focussed on developing novel fast fabrication and characterisation approaches using simplified devices and reduced fabrication processes to provide valuable rapid feedback on device performance, fabrication, design and epitaxy. Establishing and scaling up these approaches to large diameter (>100mm) wafers and disentangling the effects of fabrication from device performance in a reduced time frame can minimise the development cycle, improve product yield and reduce manufacturing costs.

Lead : Dr Craig Allford; Email: AllfordCP1@cardiff.ac.uk

Contributing academics: Prof. K. Elgaid, Dr Q. Li, Prof. H. Liu, Prof. M. Missous, Dr R. Quaglia, Dr R. Smith, Prof. P.M. Smowton, Prof. D. Wallis.

We have continued to expand the CSHub wafer-scale characterisation capabilities and tools for devices such as vertical-cavity surface-emitting lasers (VCSELs) and light-emitting diodes (LEDs). Recent additions to wafer-scale capability include: calibrated power-current-voltage (P-I-V) and high resolution rapid spectral measurements (400-1700nm) between 25°C and 200°C. In addition to this, we have also established wafer-scale electro-optic small-signal modulation response measurements for high speed devices with capabilities up to 45GHz (500nm-1630nm) or 67GHz at 1310nm and 1550nm.

Progress and challenges: Researchers at the CSHub, in continued collaboration with epitaxy wafer supplier IQE Plc and Cardiff University's fabrication facility the Institute for Compound Semiconductors (ICS), have further developed a rapid VCSEL fabrication and characterisation process. Key device performance parameters have been mapped across 150mm wafers to provide rapid feedback on the quality and uniformity of the wafer manufacturing process. Results of this work are published in the *IEEE Photonics Journal,* vol. 14, no. 3, pp. 1-10, June 2022 (doi: 10.1109/JPHOT.2022.3169032).

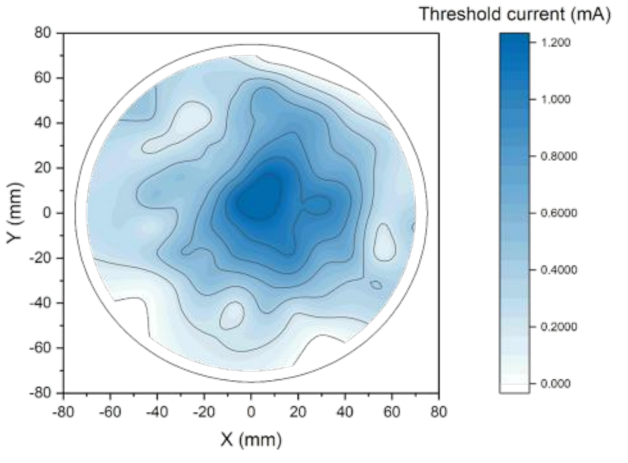
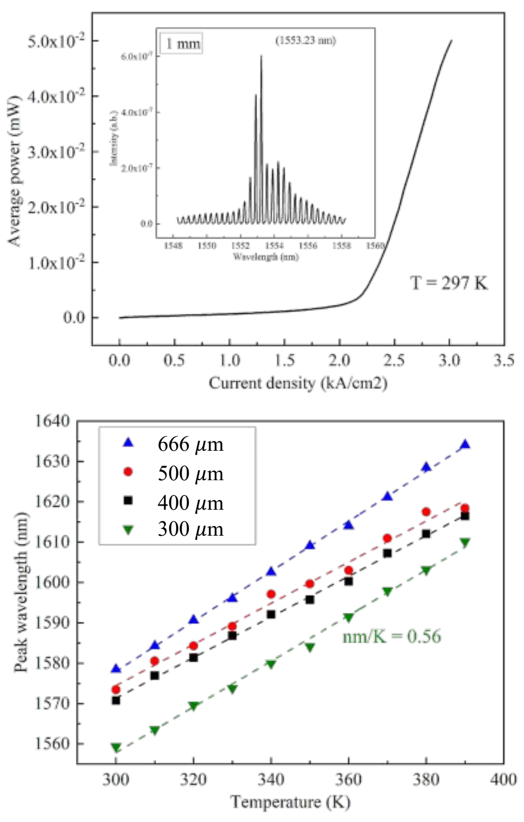


Figure 1 (above): Threshold current map of a 150mm VCSEL Quick Fabrication (VQF) wafer adapted from 10.1109/JPHOT.2022.3169032



Utilising fast-fabrication and characterisation processes developed for edge-emitting lasers hub researchers are working in collaboration with WP1 to develop C-band (1550nm) InAs quantum dot (QD) lasers for applications in next generation light detection and ranging (LiDAR), telecommunications and photonic integration applications. Grown on native indium phosphide substrates we have demonstrated excellent device performance with uncoated short-cavity lasers exhibiting ground state-lasing at temperatures >115 ° C. Presented at Semiconductor Integrated OptoElectronics (SIOE) 2022 these results demonstrate the excellent promise of this technology for delivering high performance C-band optical sources on silicon substrates via a direct epitaxy approach .

Figure 2 (left): Power vs current density of a 1mm cavity length InAs QD laser at 23°C (top) with lasing spectrum inset; Peak emission wavelength of InAs QD lasers against temperature for various cavity lengths (bottom) demonstrating excellent performance over a large temperature range.

Manufacturing Technology for Optical Data Communications on Silicon

Summary: Continuous development of high performance silicon-based InAs/GaAs quantum dot (QD) lasers has been pursued in this work package. Here, we report recent progress in the development of two-section InAs/GaAs QD mode-locked lasers. In addition, system-level optical data transmission has been experimentally demonstrated with advanced 64 Gbaud four-level pulse amplitude modulation format (PAM-4) using QD DLLs.

Lead : Prof. Huiyun Liu Email: Name: Prof. Huiyun Liu

Contributing academics: Dr Siming Chen, Dr Mingchu Tang, Dr Qiang Li, Prof. Alwyn Seeds, Prof. Peter Smowton, Prof. Huiyun Liu

In this package, we developed high performance optical frequency comb (OFC) sources based on passive two-section InAs/GaAs Quantum Dot (QD) mode-locked lasers (MLLs) with ultra-high fundamental repetition rate (~100 GHz). This has been approached via optimising the growth conditions, by which a QD active region with ultra-high dot density (>5.0 x 1010 cm-2) and good uniformity is accomplished. In the last 12 months, we have developed specially designed MLLs that favour the generation of nearly Fourier-transform-limited pulses over a wide drive current range by only pumping the gain section while the saturable absorber (SA) is left floating

Progress and challenges: The usage of OFCs as multi-wavelength light sources in high-speed dense wavelength-division multiplexing (DWDM) transmission systems has attracted increased attention, since it can potentially address the explosive growth of data traffic within data centres. At the same time, the fully exploited conventional C- and L- bands require the research on O-band to expand the transmission capacity of the existing photonic networks. It has been reported that QD mode-locked OFCs benefit from the broad inhomogeneous gain spectrum, ultrafast carrier dynamics, low threshold current, and temperature resilience [Photonics Research. 8, 1937-1942 (2020)].

High optical gain is a prerequisite for ultra-high repetition rate pulse generation in a two-section passively MLL, which is a particular challenge to achieve within an extremely short laser cavity (~ 400 µm). To this end, a novel design is utilised in the active region, where a larger than usual number of QD layers (8 layers in total) was employed to obtain the desired high optical gain. The laser cavity length was set to be 405 μm, 14% (56.7 µm) of which formed the SA section. This gives a high gain-to-SA saturation energy ratio in the MLLs.

Figure 1 shows the measured spectrum of the optical combs under bias condition of I_gain = 66 mA. A centre wavelength of 1290.755 nm with 7 potential channels within a 3-dB bandwidth of 3.46 nm is achieved; the adjacent mode spacing corresponding to a fundamental repetition rate of ~94.6 GHz. To the best of our knowledge, this is the highest fundamental repetition rate ever achieved by a single QD-MLL in telecom O-band. In addition, nearly Gaussian transform-limited pulses were observed throughout the testing range.

In this work, we successfully proved that our devices are capable of realising 128 Gbit/s/ λ PAM-4 back-to-back and 5km SSMF transmissions, as shown in Figure 2 [J. Phys. D: Appl. Phys. 55, 144001 (2022)].

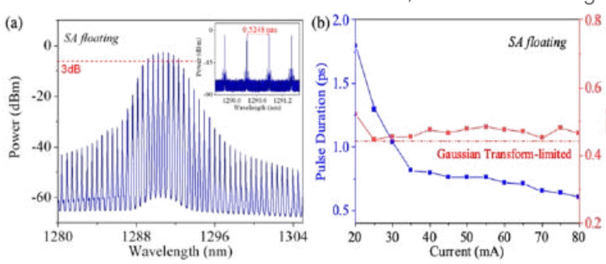


Figure 1 Room-temperature characteristics of two-section unbiased passively QD MLL with SA floating. (a) Spectrum under bias condition of I_gain = 66 mA. (Inset: high-resolution optical spectrum for adjacent channels (Resolution: 0.04 pm) (b) Measured pulse durations and corresponding calculated time.bandwidth product values in the range of I_gain from 20 mA to 80 mA.

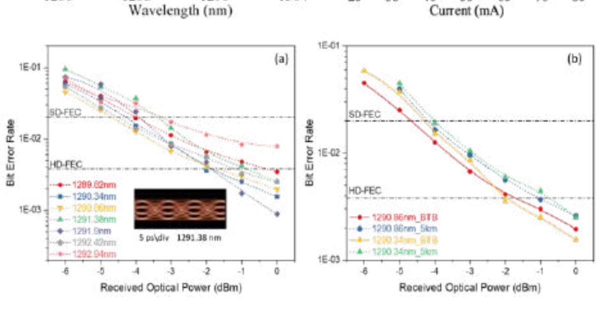


Figure 2. Light-current measurements of laser at various temperatures in pulsed mode

WORK PACKAGE 5

Advanced Radio Frequency Devices & MMICs

Summary: Building on on-going success, the aim of this work package is to demonstrate a UK GaN-on-Si GaN based HFET technology baseline. Specifically targeting wireless applications, this work package aims to ultimately establish a full GaN-on-Si HFET device, MMIC based passive devices and a MMIC technology platform suitable for high to medium power microwave 5G system applications. This work package uses high-frequency device characterisation at staged points to allow feedback for the optimisation of the epitaxial growth to deliver device performance and a fully integrated on-chip technology in line with industrial requirements. Work package activities are closely aligned with major compound semiconductor manufacturing industry partners including IQE, SPT and the CSA Catapult.

Lead: Prof. Khaled Elgaid Email: ElgaidK@Cardiff.ac.uk
Contributing academics: Prof. Paul Tasker, Dr. Johnathan Lees Dr. Roberto Quaglia, & Dr. Abdalla Eblabl
Supporting Researcher: Dr. Arathy Vargese

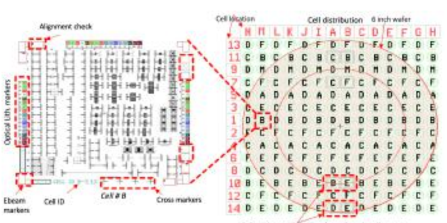
The WP5 focus is to develop advanced GaN on Si RF active and passive devices and implement them through the realisation of high-performance MMICs for wireless high data rate communications systems. The technology development in this WP is aimed at addressing industry requirements and utilising full wafer process methods. Strong links have been formed with several key industry partners in both areas of technology, such as process monitoring and verification, as well as design, where component specifications requirements are defined. Key industry interactions include SPTS, IQE, MBDA, CSA Catapult, Leonardo and IconicRF.

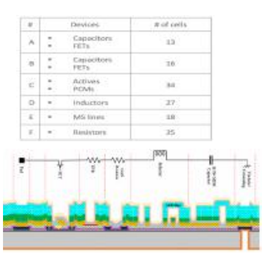
Progress and challenges

An alternative solution to RF GaN on SiC is to use GaN on Si substrates, hence large (>300mm), lower-cost and the potential of volume production. These advantages of GaN on Si come at the cost of lower performance in comparison to GaN on SiC, due mainly to losses in the substrate (challenges in the realisation of low-loss MMIC interconnect and passive structures), large lattice mismatch (larger wafer-bow and challenges in fabrication) and relatively poor thermal conductivity. Irrespective of the substrate used, to obtain high intrinsic performance RF GaN devices, there is the need to develop a short-offset gate lengths of $\leq$ 0.25um aligned in a source/drain gap of $\leq$ 5µm technology. Ensuring a corresponding increase in extrinsic performance requires RF parasitics to be minimised, optimisation of the epitaxial layer, layout optimisation, minimisation of ohmic contacts /access resistances and development a robust PDK. Advanced RF devices & MMIC technology realisation has so far been progressed in two stages; firstly by developing the necessary fabrication modules for active and passive devices on partial wafers, and then device characterisation and evaluated on different epitaxial layer structures. Now a full 6 inch wafer process now has commenced.

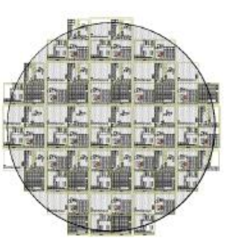
To address the key RF GaN technology development challenges, the research team have carried out essential development; reliable photo lithography for small features/gaps, an aligned gate in $\leq$ 5µm HEMT, reducing access resistance while maintaining power performance, ohmic contacts development using source/drain recess - published "Optimization of ohmic contact for AlGaN/GaN HEMT on low-resistivity silicon", 2020, IEEE TED, fabricated and characterised devices on partial wafers. Working with multiple industry partners and linking with other projects developing RF GaN on SiC (the GaNforCS project), a process development kit (PDK) is being developed to allow the simulation and design of active circuits,). Figure 1 shows a top-view of full 6-inch layout mask-set to allow for a robust PDK development. The aim of next stage of development will be based around wafer-level and PDK realisations with more involvement by industry partners.

Figure 1 shows a top view of full 6-inch layout & technology





Planned MMIC Technology



Complete mask design layout for 6'' wafers

Monolithic Integration of Micro-emitters and HEMTs for Microdisplay and Li-Fi

Summary: Building on the work in the platform our approach is to develop a direct epitaxial technique to integrate III-nitride micro light emitting diodes (µLEDs) and HEMTs on a single wafer in order to demonstrate and then manufacture monolithic on-chip integration of µ-LEDs and HEMTs for ultra-high resolution & ultra-high efficiency micro-displays and ultra-fast & zero cross-talk Li-Fi; We will continuously develop industrial compatible selective epitaxial overgrowth steps to integrate CS/Si structures with different designs on the same substrate.

Lead : Prof. Tao Wang Email: t.wang@Sheffield.ac.uk

Contributing academics: Prof. Huiyun Liu, Prof. Alwyn Seeds, Dr. Rick Smith, Prof. Peter Smowton, Prof. Khaled Elgaid.

Li-Fi exhibits striking advantages compared with Wi-Fi technology in terms of bandwidth, data transmission rate. The major component of Li-Fi is visible LEDs which need to have ultra-fast response time and need to be controlled by high frequency electronic components. The most promising approach to achieving high bandwidth and high data transmission rate for Li-Fi to utilise µ-LEDs. Furthermore, AR & VR microdisplays, smart watches and smart phones require µLEDs with an ultra-small dimension, high EQE and narrow spectral linewidth. An on-chip epitaxial integration of III-nitrides µLEDs and HEMTs on low cost and up-scalable silicon substrates for LiFi and microdisplays is the best way forward, where each µ-LED transmitters can be individually controlled by GaN based HEMTs uniquely

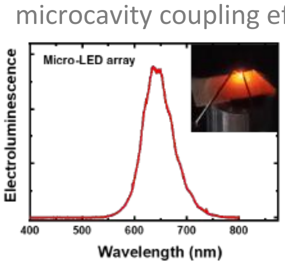
Progress and challenges: To achieve a high modulation bandwidth and a high data transmission rate, µLEDs need to be driven at a high injection current density, which is ~3 orders of magnitude higher than those for normal visible LED operation. µLEDs are traditionally fabricated by dry-etching techniques, leading to severe damages and thus a substantial reduction in performance and a great challenge to viability at a high current density. Conventional biasing generates a great challenge for a single µLED, which needs to be modulated at a high injection current density and at a high frequency.

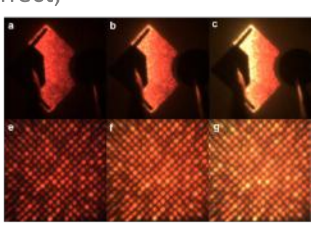
Due to the similar reasons, a heterogeneous integration approach for the fabrication of a microdisplay is far from requirements. There also exist extra two major issues: (1) a great challenge in obtaining III-nitride based red µLEDs; (2) colour instability of III-nitride LEDs with increasing injection current.

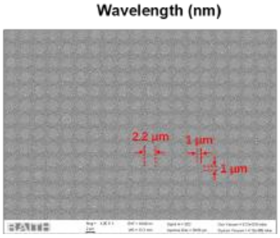
We aim to develop a direct epitaxial technology to manufacture a monolithic on-chip integration of µLEDs and HEMTs for a microdisplay with ultra-high resolution & ultra-high efficiency (> 20% EQE, ≤ 5 µm pixel and ≤ 2 µminter-pitch) and a LiFi system with ultra-fast (>2 GHz) and zero cross-talk. We also aim to establish and then develop a spinout into a global manufacturer of monolithic on-chip integration systems.

Achievements: 1) Demo ultra small red µLEDs with a record EQE at 640 nm (2 µm in diameter, 2 µm in inter-pitch and 1.75 % Max. EQE); [1]

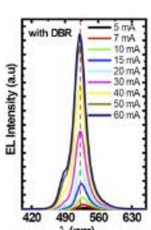
(2) Demo the 1st III-nitride µLEDs with emission wavelength stability with increasing current due to the microcavity coupling effect;[2]

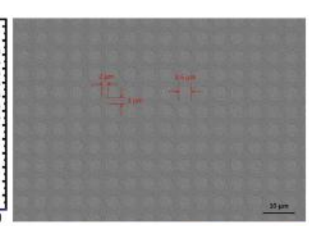


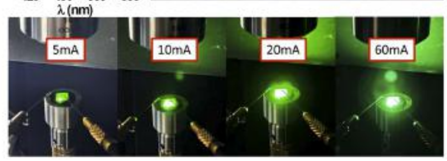




(1)Electro-luminescence (EL) spectrum of our red µLED arrays, showing strong emission at 642 nm; (2) SEM plan-view image; (3) EL emission images taken at different injection current under different magnifications







An approach to epitaxially integrate µLEDs and a microcavity allows the emission from the µLEDs to be coupled with the microcavity, leading to a negligible shift in emission wavelength with increasing injection current.

References:1."A simple approach to achieving ultrasmall III-nitride µLEDs with red emission", ***ACS Appl. Electron. Mater.*** (accepted)

2. "A simple approach to mitigate the emission wavelength instability of III-nitride µLED arrays", ***ACS Photonics*** (under review)

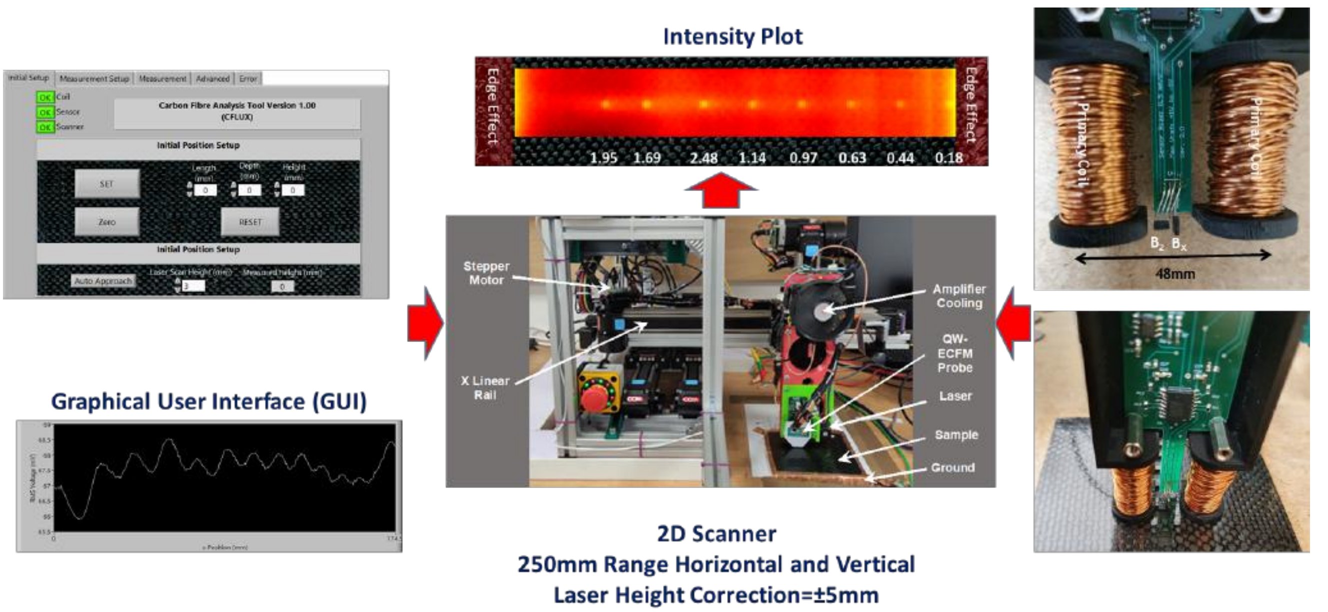
Magnetic Arrays

Summary: The approach is the integration of high electron mobility, high magnetic sensitivity 2DEG structures with on board analogue and digital electronics to deliver scanning magnetic imaging systems for Non-Destructive Testing of metallic and composite materials

Lead : Prof M.Missous Email: .missous@manchester.ac.uk

Contributing academics: Dr M. Migliorato

The overarching theme of WP7 is magnetic imaging of ferrous and non-ferrous materials and lately composites. The work follows a vertically integrated approach starting from epitaxial growth of advanced 2DEG structures with tailored magnetic sensitivities to device fabrication of integrated arrays and passives, packaging and finally system integration for imaging of flaws, defects and microstructures (See Figure 1).



Progress and challenges: During the period magnetic imaging modality using Quantum Well Hall Effect sensors (QWHE) for were extended to study composites including both physical defects and fiber detection and imaging (Figure 2) using a novel technique we term QW-ECFM. We have designed and delivered numerous system demonstrators with key challenges being imaging and classifications of flaws and defects in metals and composites.

Impact has been very strong as demonstrated in 6, separate, fully funded collaborative INNOVATEUK projects with [Renishaw, TWI, EtherNDT, FarUk, Wright, Home office, BAESystems] in imaging corrosion under insulation in steel and flaws and fibers in composites.

The work to date in WP7 has now extended from ferromagnetic (and non-ferromagnetic) to composite materials to detects flaws and microstructures spanning the frequency range 50Hz to 2MHz.

The work on composite materials uses conductivity as the imaging modality which has necessitated the use of very high frequency (MHz) interrogation techniques. The high frequency techniques also result in much more compact imaging systems that are ideal for aerospace applications.

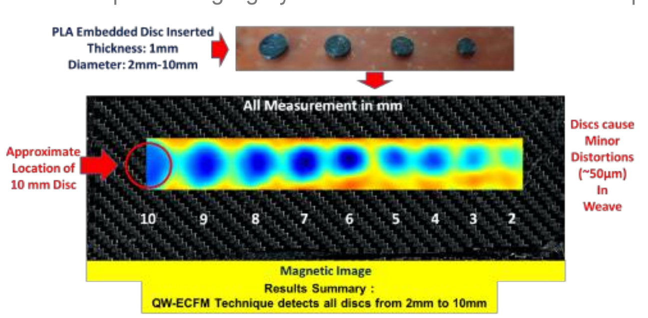


Figure 2 QW-ECFM Technique detects of embedded discs in a composite matrix.

Generic Photonic Integration

Summary: The aim of Work Package 9 is the development and progress of generic photonic integration in optoelectronics devices and systems. Photonic integration allows multiple optical devices to be fabricated on a single chip, which in turn aids the realisation of monolithic integration technologies in addition to the smaller size, lower cost and higher efficiency and reliability. Overall, photonic integration technologies drive the development of next generation high performance devices for data communications and biomedical applications

Lead : Dr Yun Long; Email: longy11@cardiff.ac.uk

Contributing academics: Peter Smowton, Huiyun Liu, Michael Wale, Pawan Mishra, Sara Gillgrass

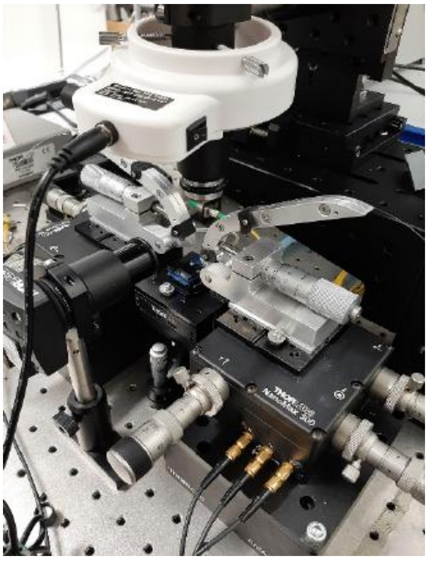


Figure 1: Photograph of passive building block test bed including semi-automatic alignment.

Our approach to optoelectronic integration is based on a quantum dot active material. Such material must enable a variety of active functions such amplification and detection and also passive functions such as waveguides, splitters and combiners. Quantum dot material is well suited to producing emission and absorption over a wide wavelength or frequency range while operating a relatively low current. Passive functions are more difficult and progress is required on solutions to reducing loss. We are working with approaches using either ion bombardment or selective area intermixing. Currently Silicon is one of the most popular materials used for manufacture of photonic integrated circuits due to its abundance, thermal and chemical stability, ease of manufacture and the existing manufacturing infrastructure. InP based photonic integrated circuits on the other hand have the benefit of intrinsic active building blocks although other aspects are not as favourable. In WP9 we are exploring the relative advantages and the practicality of manufacturing an integrated subsystem for Optical Coherence Tomography (OCT) using the GaAs based approach comparing and contrasting with work done on an associated project on silicon / silicon nitride and with published work using InP.

Within the integration process, a broad range of functionalities can be realised from basic building blocks (BBBs) which control light propagation such as amplifiers, modulators and waveguides. A variety of circuits and systems can be realised through connection of these building blocks in a variety of topologies, a process known as generic photonic integration. In chip design, generic integration processes can be enhanced through the development of a Process Design Kit (PDK) with component libraries containing accurate models of building blocks, which will lead to a reduction of the design time and costs necessary to achieve the required performance. This work package will also work towards such a Process Design Kit for optoelectronics systems based on a GaAs platform.

Progress and Advancement:

- Construction of test bed for measuring losses in passive building blocks and integrated circuits.
- Finalised list of requirements for PDK towards the realisation of an OCT system based on GaAs for comparison to alternative approaches based on Silicon/Silicon Nitride.
- Fabrication and evaluation of initial active devices
- Designs commenced for building block components using Photon Design

Rounds 1, 2 and 3

During the Hub's second year, we released our first call for applications to our feasibility study fund. This fund, totalling £1M (full economic cost) was reserved for new studies which push the boundaries and contribute to the strategy of the Hub. The aim of funding these feasibility studies is to broaden the reach of the Hub by encouraging new academic and industry partnerships, whilst supporting new cutting-edge research which is complementarity to and aligns with Hub objectives.

We originally envisaged supporting up to 10 projects of average length of 7.5 months; however we have used the flexibility available to us to set out a more extensive strategy for engaging with new partners and delivering key performance indicators via feasibility study funding.

Funding plan

Round 1, the studies funded during which have concluded, called for applications of up to £40k (80% full economic cost) over 6 months. This was followed with an opportunity for successful round 1 studies to apply for up to £96k (80% full economic cost), with this funding intended to lead to and facilitate a large scale EPSRC or Innovate UK grant application with strategic alignment to the Hub. These studies would build on successful feasibility studies and deliver additional key performance indicators for the Hub.

This was followed by a third funding round, coordinated with funding calls from other future manufacturing Hubs in order to encourage the possibility for collaborations involving multiple Hubs. This provided an opportunity to apply for up to 50k (80% full economic cost). This final call invited new applications from areas that overlap between the Hubs, strengthening the links amongst them and promoting interaction, as well as delivering value for money.

Evaluation of applications for funding

The Hub Management Board (MB) hold responsibility for awarding funding for feasibility studies and have taken the advice of the Hub's Strategic Advisory Board in assigning funding to applicants. Applications for the first round of funding were prioritised for funding according to the delivery of new academic and industrial collaborators, and were then scored on:

- Scientific Quality and Clarity
- Potential Impact/Opportunity
- Hub Alignment

These criteria were used to enable new academic collaborators to request funding for new and innovative research projects which were aligned to the Hub strategy.

Funded applications

Six studies were awarded round 1 feasibility study funding. They began their journey with the Hub in August 2018 and were 6 months in duration. The Hub invested £229,992 in the novel studies and details of each feasibility study can be found in the Hub's 2019 annual report: https://compoundsemiconductorhub.org/downloads

In the second round, to enable the most promising of these studies to continue their work with the Hub, 4 continuation studies were awarded funding and their studies commenced between August and October 2019, with durations between 12 and 18 months. The Hub invested £376,806 in the continuation studies and details of each continuation study can be found in the Hub's 2020 annual report: https://compoundsemiconductorhub.org/downloads

In the final round, the Hub invested a further £247,799 in 5 new studies as part of a joint feasibility call with other future manufacturing Hubs. These projects started from April 2020 onwards, with a duration of 6 months although all projects have incurred delays due to Covid. The studies are listed below and descriptions can be found on the pages that follow this.

£229,992 Invested in initial 6 feasibility studies

£376,806 Invested in 4 continuation studies

£247,799 Invested in 5 new feasibility studies

£854,597 Total investment

2020 Hub-funded feasibility studies

PI	Insititutions	Title
Dr Philip Shields	University of Bath	Manufacturing of large-area InP on nano-V-grooved CMOS-compatible Si
Dr Kean Boon Lee	University of Sheffield	Novel GaN-based Vertical Transistors for LED Driver Applications
Dr Nicolás Abadía	Cardiff University	Measurement of Carrier-Induced Electro-refraction in InAs/In(Ga)As Quantum Dots
Dr Antonio Hurtado	University of Strathclyde	Vertical-cavity LASER arrays for BRAIN-inspired photonics (LASERBRAIN)
Dr Vishal Ajit Shah	University of Warwick	Semi-insulating SiC epitaxy on SiC and Si substrates, for monolithic integration of GaN "on insulator" RF technology and high voltage SiC devices.

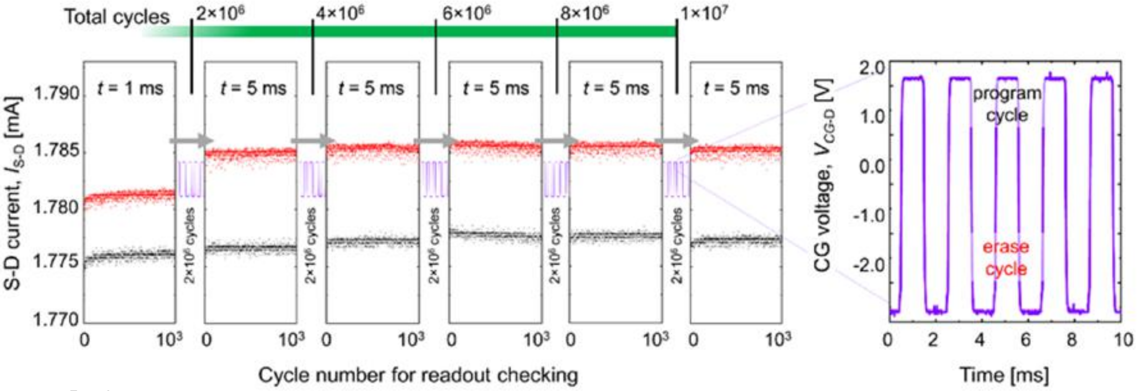
The 2020 feasibility study: Measurement of Electro-refraction in Quantum Dots study, led by Dr. Nicolás Abadía has been delayed due to Covid and facilities not being able to grow wafers. The project aims to verify strong electro-refraction in quantum dots experimentally. This research will enable more efficient phase shifters to improve Mach-Zehnder Interferometers, and there will be more information on the project's research in next year's annual report.

Towards compound semiconductor non-volatile RAM manufacture on Si substrates.

Lead applicant: Prof. Manus Hayne, Lancaster University.
Partners: University of Warwick, IQE plc, EM Analytical, IMEC zvw.
Hub Mentor: Prof. David Wallis

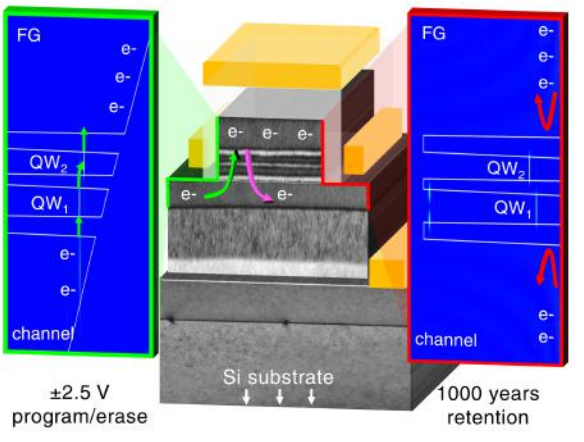
Summary: The memory chips at the heart of all computers and electronic devices – known as dynamic random access memory (DRAM) – are fast, but volatile, meaning that information is lost unless it is refreshed multiple times per second. Furthermore, when data is read from DRAM it is destroyed (destructive read), and needs to be reprogrammed, which is inconvenient. In this project we are working on a completely new type of memory, ULTRA**RAM**™, which fully exploits the opportunities for quantum engineering of materials and devices that are available in the compound semiconductor family. ULTRA**RAM**™ memories are expected to be as fast as DRAM, but are non-volatile and with non-destructive read. Computers and electronic gadgets of the future using ULTRA**RAM**™ would be fast, boot-free (instantly on or off) and consume significantly less power.

Outcomes/major findings: The primary outcome was the successful implementation of the active layers of the memory on Si substrates, overcoming multiple materials issues such as the 12% lattice mismatch between Si and the compound semiconductors used (GaSb, InAs and AlSb). Most remarkably, devices on Si substrates actually out-performed previous generations on GaAs, showing extraordinary (extrapolated) storage times of at least 1,000 years, and a program/erase (P/E) cycling endurance of at least 10 million, which is two to three orders of magnitude better than flash. P/E switching times were as low as 1 ms for our relatively large devices with 20 μm feature sizes, implying that, with capacitive scaling, 1 ns switching should be achievable at 20 nm node. Due to ULTRA**RAM**™'s small capacitance and low switching voltage of 2.5 V, its switching energy per unit area is 100 times lower than DRAM and 1000 times lower than flash. This work was published in Advanced Electronic Materials where it was featured on the back cover of the April 2022 issue.



After 10^7 P/E cycles there is no discernible degradation in the ULTRA**RAM**™ 0/1 memory window.

Relevance to manufacturing: The development and commercialisation of a new memory technology is a gargantuan task. ULTRA**RAM**™ has been tested in single device (bit) format, with 2x2 array fabrication in progress. Achieving cost-competitive manufacturing requires shrinking the devices to the nanoscale, exponentially increasing the number of bits on a chip, and implementation on industry-standard 300 mm Si wafers that are compatible with microelectronics chip production facilities. We have successfully demonstrated implementation on Si substrates, which is a major milestone on the path to manufacturability. Device scaling and larger arrays will be investigated with separate funding, with a target of 64-bit arrays at ≤100 nm node in 2024. The ambitious medium-term aim is a 1 Mbit array on Si with integrated III-V CMOS addressing logic.



Composite figure showing transmission electron microscopy image of the compound semiconductor layers, device structure and resonant tunnelling principle of ULTRA**RAM**™ operation.

Angled-Cage Etching of Semiconductors (ACES).

Lead applicant: Prof R Taylor, Oxford University.
Partners: Cambridge University (Prof R Oliver), Cardiff University (Dr J P Hadden, Prof A Bennett, Dr D Beggs), Seren Photonics (Dr B Humphreys) and Poro Technolgies (Dr T T Zhu).
Hub Mentor: Prof. P Smowton

Summary: Gallium nitride (GaN) is a commercially important semiconductor with widespread use in solid state lighting, blue lasers, and high speed and high-power electronics. We have developed an inductively coupled plasma etching technique using a Faraday cage to control the angle of etching for gallium-nitride. The angle of the Faraday cage, the gas mix, and the etch chamber conditions define the angle of the etch and the cross-sectional profile of the semiconductor. It is possible to achieve undercut angles of up to 45 degrees and, if etched to sufficient depth, one can completely release the structure. We fabricate singly- and doubly-clamped suspended cantilevers of a triangular cross section that support single optical modes in the telecom C-band.

Outcomes/major findings: The primary outcome was the study of the etch parameters required to control the etch angle and fidelity [1]. As a result of this we obtained a reproducible etch process that could create beams with the cross section of an equilateral triangle. A detailed theoretical study was made of nanostructures to couple light in/out of the nanobeams [2] which resulted in test structures shown in Fig 2a. Further investigation was made of the use of a conical Faraday cage with can be used to create structures with rotational symmetry, such as microdiscs and inverted cone Mie-resonators, as shown in Fig 2b.

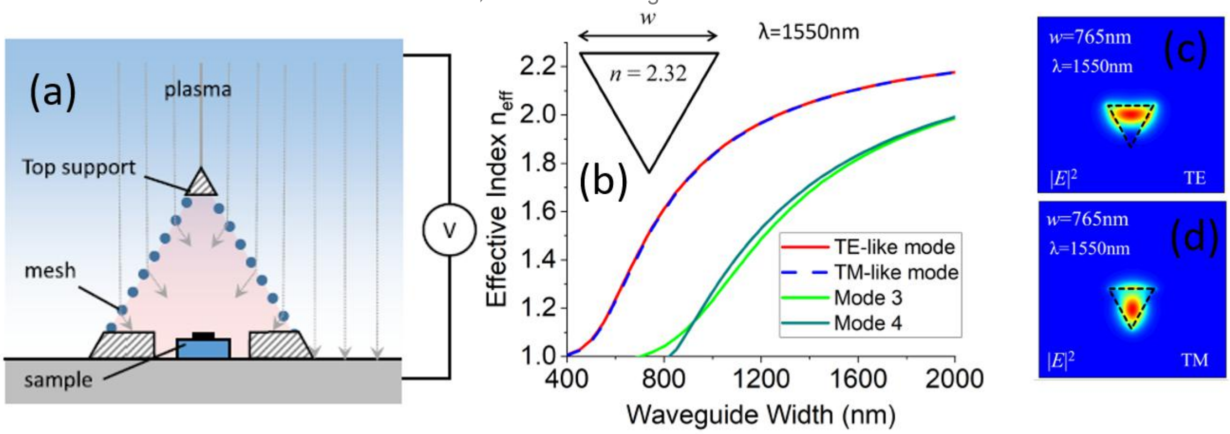


Figure 1: (a) cartoon of the cage cross section used in the etch process. (b) simulation of the guided modes effective index in a triangular beam. Single mode operation is achieved below 760nm width at a wavelength of 1550nm. Electric field distribution of the (c) TE and (d) TM modes at 1550nm.

Relevance to manufacturing: The project aligned with the Hub activities by focusing on the processing of a commercially important semiconductor. The project brings in expertise in GaN from Oxford and Cambridge Universities to the Hub, with support from Seren Photonics Ltd. and Poro Technologies Ltd. A large fraction of resources was devoted to the Institute for Compound Semiconductors' cleanroom. These activities created ICS-know-how to the benefit of all Hub partners. The data from the feasibility studies was used to support the Fellowship application of Dr JP Hadden (Ser Cymru Fellowship, 2020-22) and Prof A Bennett (EPSRC Manufacturing Fellowship, 2020-2025).

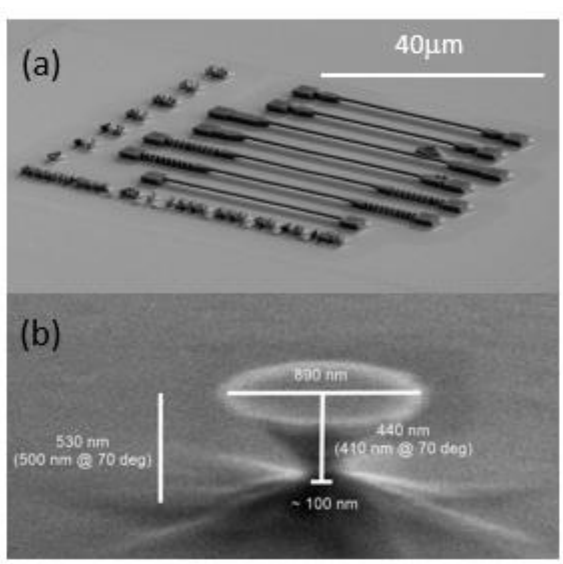


Figure 2: SEM images of Faraday cage etched GaN nanostructures. (a) using a linear cage to create suspended nanobeams between novel couplers (b) using a conical cage to create Mie resonators with cylindrical symmetry.

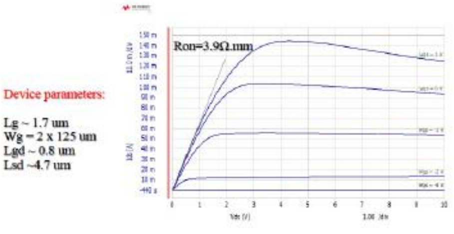
[1]G. Gough et al, AIP Advances 10, 055319 (2020).
[2] J. Hadden et al, In preparation for J. Phys D Special Issue.

Novel Fast-Turnaround GaN Epitaxy Assessment – Quantitative Demonstration of Benefits

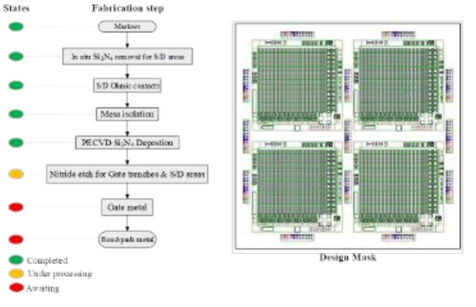
Lead applicant: Prof Martin Kuball, University of Bristol
Partners: IQE, IconicRF
Hub Mentor: Prof. Khaled Elgaid

Summary: The project aim was to demonstrate a physics-driven validated methodology for current-collapse vulnerability assessment of RF GaN HEMT devices using a short-loop process requiring a few days. The aim was to demonstrate this approach by applying the substrate ramp technique to a systematic design-of-experiment matrix of structures supplied by IQE, processed by CSC, and validated by IconicRF. The result would be a rapid optimization of the GaN-on-Si epitaxy of direct benefit to the Hub and IQE, together with a highly publishable physical model which justified the optimum configuration.

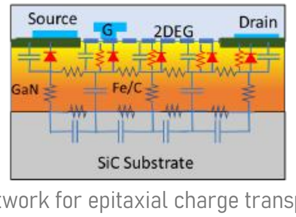
Relevance to manufacturing: GaN HEMT devices are susceptible to reversible charge trapping under transient conditions leading to a phenomenon known as current collapse. This leads to a serious reduction in output power, and a time dependent modulation of the power which impacts linearity in applications such as basestation power amplifiers. A major part of the trapping occurs in the semi-insulating epitaxial layer under the 2 dimensional electron gas conducting channel, and it is currently impossible to predict the performance of an epitaxy in RF devices without the expensive and highly time consuming fabrication of a complete active device. Previous work at the University of Bristol showed that the trap dynamics was associated with the combined effect of unintentionally incorporated background carbon impurities and vertical conducting dislocations. Bristol had also developed a straightforward electrical approach to characterising the trapping performance of the epitaxy based on a short-loop simple device structure which could be fabricated in a fraction of the time to make a full device, This would deliver major benefits for manufacturers by fast validation of new epitaxial variants with benefits for both the epitaxy grower and the device fabricator. The project aimed to validate this approach by fabricating multiple short-loop processed devices using epitaxy from IQE, fabrication at the CS-Hub, and testing at Bristol. A final full transistor batch was intended to be fabricated with full RF testing at IconicRF.



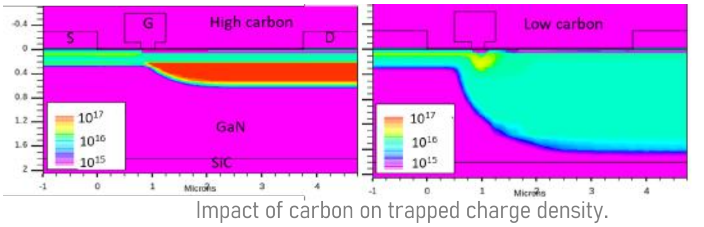
Short-loop transistor characteristic.



Process flow and maskset.



Network for epitaxial charge transport.



Impact of carbon on trapped charge density.

Outcomes/major findings: IQE grew an initial set of epitaxial variants, a short-loop maskset was designed, and processing initiated at CSC. The project successfully implemented and established a short-loop HEMT device process in the Hub. However fabrication was seriously impacted by COVID, and as a result the planned multiple process loops did not occur, and validation of the impact of epitaxial variants on device performance was not undertaken. However the understanding of the mechanisms for current-collapse that emerged in the early part of the project were implemented in device simulations at the University of Bristol. These were able to predict the impact of dislocations / carbon impurities on key device parameters. These results were presented at international conferences in Japan and the USA and published in an invited paper in J. Uren and Martin Kuball 2021 Jpn. J. Appl. Phys. 60 SB0802.

Annual and long-term targets to measure success

The CS Hub has a number of targets formed of measurable research outputs that are carefully designed to measure the success of the Hub in the context of the CS research environment. Many of these targets are only possible to achieve in the long-term, while others can demonstrate more immediate success for the Hub. The Key performance indicators (KPIs) for the Hub are detailed below. The following page contains some of the Hub's key achievements for these KPIs.

KPI	Success criteria
New industrial partners, based on exciting manufacturing challenges	5 per annum
New universities joining	5
Close collaborative links with other EPSRC Manufacturing Hubs and the EPSRC Centre for III-V Technology	Joint activities / events
Close collaborative links between the hub and major complementary overseas centres of excellence such as MIT, IMEC or NTU Singapore	2 over duration of Hub
Compound Semiconductor training centre activities to include: a) university and industry funded doctoral level training, b) MSc courses c) on-job and/or apprenticeship training to support industry d) summer schools for postdocs and PhD students	Delivery of a number of training activities per annum
Research and industrial awards per year for associated activity	Average of £5.5M (100% FEC) per annum
Conference presentations per year	Average of 10 per annum
Publications per year	Average of 20 per annum
Commercial impact activity to include: a) Number of IP disclosures/patents filed. b) Number of IP licences granted. c) Amount of VC funding generated, based on Hub technologies. d) New product roll-outs from partners, based upon Hub technologies. e) Sales value enabled by Hub technologies.	This is a late/lagging indicator and can be used later in the project to monitor success.
Outreach activity to include training	Delivery of a number of outreach activities per annum
Career development of Hub staff	Demonstration of staff development via securing fellowships, career training, etc.

THE HUB IN NUMBERS

Based on our Key Performance Indicators, and some other important measures of success, we have generated some impressive numbers at the Future CS Hub.

132 Publications

183 Conference presentations & abstracts

89 Collaborations & partnerships

An additional 5 are currently in negotiation

42 Further funding

49 Outreach & engagement

Including industrial events, international seminars and conferences.

35 Training activity

10 Impact

Including 1 spin off company and 7 patent applications.

17 Career development

26 Links to other hubs and centres overseas

HUB OUTREACH

STEM Ambassadors

We see increasing opportunities for face-to-face outreach activity over the coming year. The Hub has begun coordinating with our cluster partners to train Hub researchers as STEM ambassadors, with a focus on working with schools at different key stages to promote the importance of compound semiconductors and related careers.

Hub engagement with Industry

Over the past year we have continued to work with our industry partners in several ways and in accordance with TRL evolution of the Hub's work. This includes engaging with key partners such as the Welsh Assembly Government; industry partners providing PhD sponsorship for Hub students; and strategic partnerships to support specific elements of Hub research.

Hub Website and Twitter

The content and structure of the Hub website (http:/compoundsemiconductorhub.org) has been updated over the last year and now includes several new areas to make content and Hub services more accessible. Twitter remains a key communication channel for the Hub (@FutureCSHub) and we now how have over 441 followers. We effectively use Twitter to promote Hub news and interact with audiences for events such as SIOE. The website also facilitates to the public facing videos described below.

About The Hub

Hub Research

Latest Hub News

Conferences

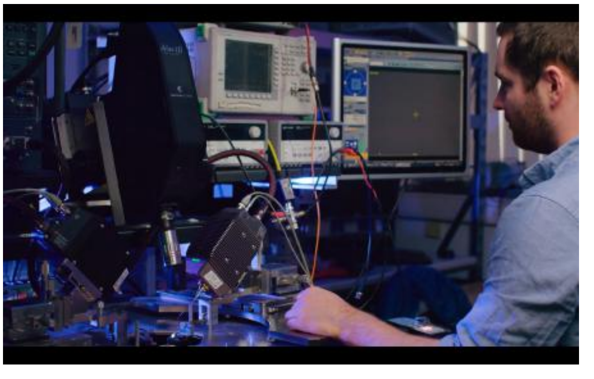
The Hub was represented at major international conferences such as Photonics West 2022, Photonics Europe 2022 and CS Mantech 2022. In April 2022, the CS Hub ran the Semiconductor and Integrated Optoelectronics Conference (SIOE) welcoming participants from across the UK and continental Europe.

Training

The Hub commissioned Rockadove, overseen by Grace Mullally the then Hub outreach officer, to produce training videos featuring Hub staff on topics such as wire bonding and mounting Compound Semiconductor chips with a view to provide alternative training modalities.

Videos

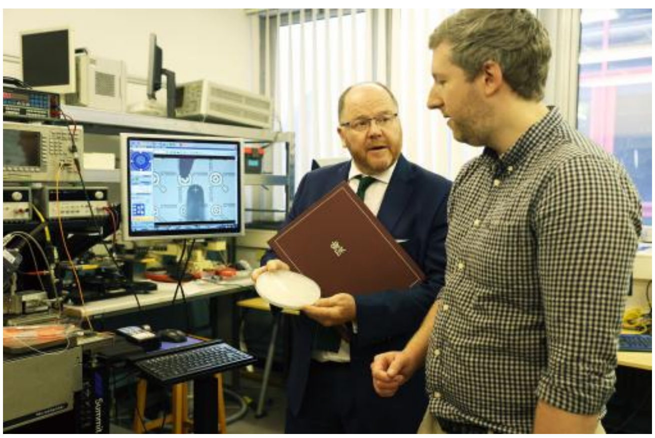
Videos explaining the role of the Hub, capability and mechanisms for interaction were commissioned with video production company Rockadove and featuring Hub staff and industry partners. Screenshots from videos are shown below:



Dame Professor Ottoline Leyser, the CEO of UK Research and Innovation (UKRI) visited Cardiff University on the 10th December 2021 and was briefed on the Future Compound Semiconductor Manufacturing Hub, its interaction with the EPSRC funded Compound Semiconductor Manufacturing Centre for Doctoral Training and the important role the Hub played in the creation of the Compound Semiconductor Cluster in South Wales. Dame Ottiline was also shown the current Institute for Compound Semiconductor (ICS) cleanroom and plans for the new ICS cleanroom (that has recently been handed over by the builders).

HUB OUTREACH

George Freeman, MP, was briefed on the value of the UKRI and EPSRC funded Hub and discussed the formation of innovation clusters during his visit to the Hub. George is pictured with Hub members, Peter Smowton, Angela Sobiesierski, Wyn Merdith and Craig Allford and CU PVC Research Roger Whitaker



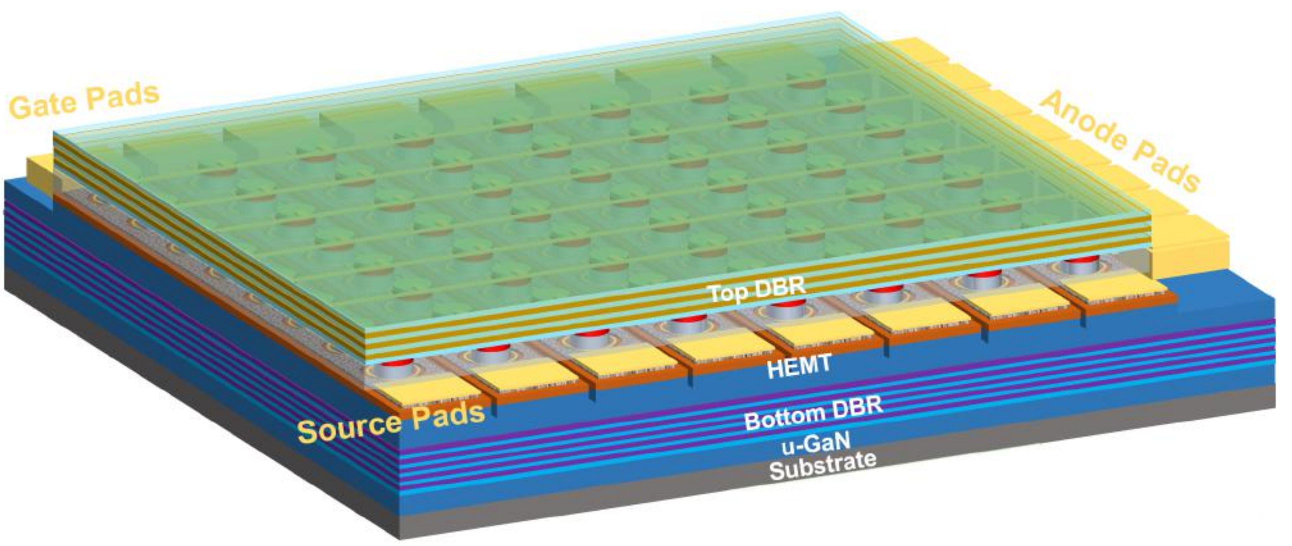
Monolithic on-chip integration of microscale laser diodes (μLDs) and electronics for micro-displays and visible light communications

The Sheffield team leads a 4.5-year international collaborative programme with Harvard and MIT in the USA and the University of Strathclyde and the University of Bath in the UK to develop the next generation micro-display systems and visible light communication systems.

Micro-displays are the key component for smart watches, smart phones, augmented reality/virtual reality (AR/VR) devices, etc. VLC technology has the potential to offer more than three orders of magnitude larger modulation bandwidth and 100s faster data transmission rate than Wi-Fi or 5G and can be used where radio frequency emissions are controlled or do not work such as in aircraft, hospitals, underwater and hazardous environments. Currently, both these technologies are based on III-nitride visible microLEDs, which are far from ideal in terms of resolution, quantum efficience, cross-talk, modulation bandwidth, data transmission rate, etc.

This programme builds on previous work by the Sheffield team which have demonstrated ultra-small microLEDs with a record quantum efficiency and have invented technologies to monolithically integrate photonics and electronics on a single chip. One of the twelve collaborations announced by UKRI the aim of this programme is to develop a novel epitaxy integration technology using micro laser diodes and electronics in order to achieve the next generation micro-display and VLC systems.

The global micro-display market has been predicted to reach $4.2 billion by 2025 and the VLC market is expected to exceed $8 billion by 2030. This programme, which is funded via an EPSRC Centre to Centre Research Collaboration scheme, is also supported by global companies such as Microsoft, Sony, etc.



Professor Tao Wang, Principal Investigator for the programme, added "The significantly increasing demands on microdisplays are pushing the requirements for ultra-high resolution and ultra-high efficiency. Several fundamental challenges with fabrication and electrical driving methods cannot be met by existing technologies therefore a disruptive technology needs to be developed. Unlike any existing photonics and electronics fabrication approaches, our research will explore a completely different approach to monolithically integrate microscale laser diodes and high electron mobility transistors on a single chip."

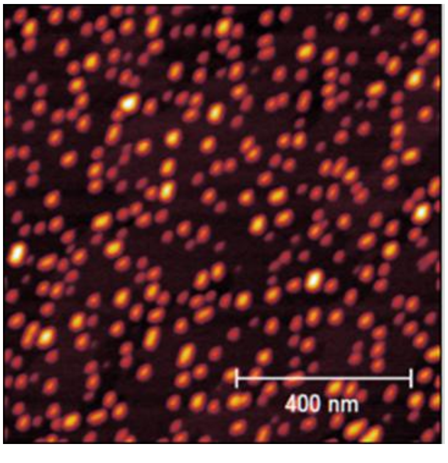
C-band quantum-dot lasers on monolithically grown Si platform

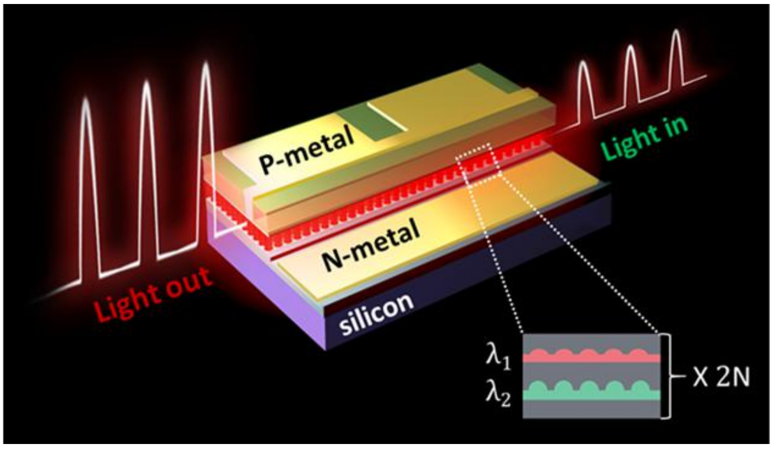
Researchers from Cardiff University and University College London (UCL) have been awarded a three-year EPSRC Grant to integrate high-performance lasers and amplifiers operating at the strategically important C-band at 1550 nm onto the silicon platform. This research aims to provide a route to scalable and manufacturable Si photonics products for long haul communications, inter-data centre connection and 3D imaging and sensing applications, removing key roadblocks and building UK's competitiveness through close partnership with industry partners.

From telecommunications to sensing applications, photonics plays a crucial role in our daily lives. The COVID-19 pandemic further highlights the importance of healthcare monitoring and remote working using high speed broadband connections. The team from Cardiff University and UCL will exploit the unique properties offered by quantum dots to develop 1550 nm lasers and amplifiers, one of the most critical components underpinning optical communication technologies.

Cardiff University and the UCL group are renowned for its current strength and historical legacy of research on quantum dot laser development. The team has demonstrated the world's first practical electrically driven 1300-nm (O-band) quantum dot laser directly grown on a Si substrate, which has changed the approach taken by the scientific and industrial community worldwide. The new grant will enable the team to build on their previous success to open up new frontiers, strengthen the UK's leading position in this important area and continue to push the technology towards application.

This project will utilise the state-of-the-art metal organic chemical vapour deposition (MOCVD) facility at Cardiff University and the molecular beam epitaxy (MBE) facility at UCL for epitaxial growth, while complementary expertise and facilities are available for device fabrication and characterisation at the Institute for Compound Semiconductors and the London Centre for Nanotechnology (LCN). Dr Qiang Li, Principal Investigator for the project, added " We will incorporate manufacturable nanostructures as the gain medium to realise advanced devices surpassing state-of-the-art. This can only be achieved by breaking the limitations imposed by reliance on a single growth technique. Sharing the know-how and experience and combining steps between MOCVD and MBE could provide important insights and enable success in meeting the major growth challenges."



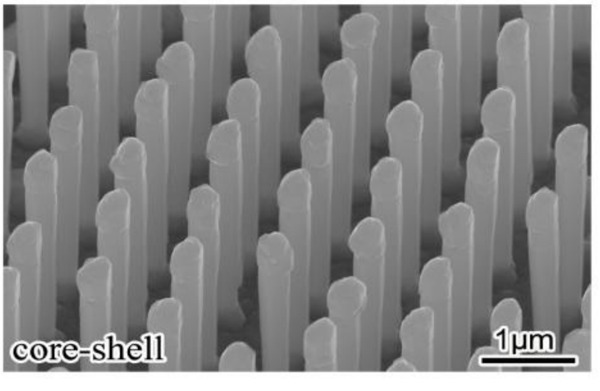


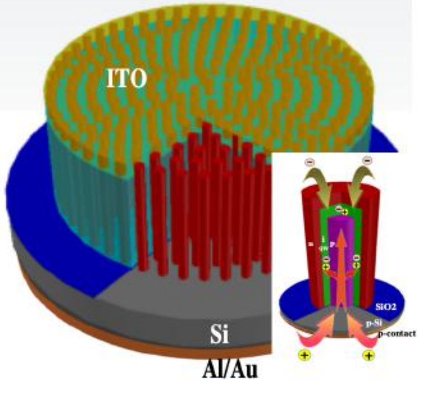
Nanowire visible and near-infrared miniature photon emitters

A new EPSRC grant – "Phosphide-based nanowires for visible and near-infrared miniature photon emitters" has been awarded to Sheffield University, UCL and Warwick University to develop micron and sub-micron visible and near infrared emitters for applications including displays, imaging and sensing. The project will comprise an extensive programme of growth development, optical and structural characterisation and device fabrication using the complementary expertise in the field of nanowires (NW) of the three institutions. GaAsP and related NW systems offer significant advantages, including direct band gap access to the critical green spectral region, easy incorporation of efficient surface passivation and a strain state advantageous for laser operation.

Semiconductor NWs provide a radically different paradigm to conventional planar growth. The small NW-substrate contact area allows growth on non-native substrates, including Si, and their small diameter allows the incorporation of larger misfit strain, providing significantly more dissimilar material combinations and giving an important extra parameter in bandgap engineering. High surface to volume ratios can be tolerated, and hence smaller device sizes, as efficient surface passivation can be added as part of the epitaxial growth.

The Sheffield, UCL and Warwick groups offer complementary expertise and a history of strong collaboration in the field of quantum dot (QD) laser development and, more recently, NW growth and characterisation The project will utilise the state-of-the-art MBE growth facility established through a £5.5M UCL Si photonics investment for the integration of III-V nanostructures with the Si platform. The UCL group have a world-class twin MBE system, the only one in the UK and rare worldwide, able to grow both III-V and group-IV materials, as required for both Si substrate pre-treatment and NW growth. The project will further utilise the £24M microscope facility at Warwick, containing a suite of ultra-stable rooms with the high environmental control required for the operation of state-of-the-art electron microscopes. Sheffield has comprehensive optical characterisation capabilities and extensive experience in the use of Nextnano simulations to model and optimise the electronic properties of complex nanostructures.





This nanowire emitter project builds on previous work by team members which demonstrated nanowire arrays on patterned Si substrates, as shown in the left image. This project will be focused on the development of electrical injection of single and multiple nanowire emitters as shown the right image.

Overview

Following the relaxation of COVID-19 regulations, we were very pleased to announce that SIOE 2022 would take place in person after last years successful online conference.

The 35th SIOE conference was successfully brought an exciting programme over 3 days, taking place predominately at Cardiff University's new Centre for Student Life. Over 120 delegates enjoyed wide range of topics from from 62 presentations covering a wide range of expertise, including: Materials Development and the impact of materials innovations on devices; Components for Integration / Integration Platforms; VCSELs and Growth

Professor Kai May Lau

We were delighted to welcome invited speaker, Professor Kei May Lau from The Hong Kong University of Science and Technology. Professor Lau gave an insightful and thought-provoking talk on lasers and photodectors on SOI by selective lateral epitaxy.

The conference dinner also returned, being held in historic Cardiff Castle. This provided a relaxed atmosphere to discuss the topics of the day and and offer opportunity to network and connect with new colleagues, for both presenters and delegates.
A careers session was provided for presenters and delegates at a drink's reception to highlight current job opportunities in the compound semiconductor sector as well as career progression and further education opportunities.

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Peer reviewed publications are a key indicator of our research success

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RESEARCH OUTPUT: PUBLICATIONS

- Semi-polar InGaN-based green light-emitting diodes grown on silicon. Shen S, Zhao X, Yu X, et al. Physica Status Solidi A. 2019: DOI: 10.1002/pssa.201900654
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