



CS Hub

Future Compound Semiconductor Manufacturing Hub

*Establishing the UK as the
primary global CS
research and
manufacturing hub*

The Future Compound
Semiconductor
Manufacturing Hub
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Annual Report 2020



EPSRC Future Manufacturing Research Hubs

compoundsemiconductorhub.org
@FutureCSHub



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Welcome message

The last year has been an exciting one for the CS Hub (<http://compoundsemiconductorhub.org/>; @FutureCSHub), as we continue to work toward our goal of establishing the UK as the global centre for CS research and manufacturing.

The Hub started as a partnership between Cardiff University, the University of Manchester, the University of Sheffield, University College London and 24 original industrial backers. Through feasibility and follow on funding we have added contributors from the Universities of Bath, Bristol, Cambridge, Lancaster, Oxford, Strathclyde and Warwick and now actively engage with over 30 industrial partners and other organisations including other Manufacturing Hubs and centres of critical mass such as the EPSRC National Epitaxy Facility.

We are addressing long term research challenges and in the past year have made significant progress in epitaxially manufacturing compound semiconductor electronic and photonic structures on silicon, in magnetic imaging systems for non-destructive testing, in the development of fast-fab (for rapid feedback on CS device performance) and in GaN micro-LEDs and integrated HEMTs.

In 2019 our partner activity, the EPSRC Compound Semiconductor Manufacturing Centre for Doctoral Training opened its doors to its first cohort of students and these students start the research project part of their PhDs next year in close collaboration with UK industry partners.



Next year will also see the Hub carrying out its first survey of industrial partners to better understand their training needs and we will incorporate these ideas into the training provided for our staff and students. We will also be continuing to work closely with our industrial partners to shape our research and make sure our outputs best connect to their needs.

It is gratifying to see Hub work seed a number of ongoing research directions including for example that on angle cage etching described on page 29 seeding an EPSRC Manufacturing Research Fellowship

A handwritten signature in black ink, appearing to read 'P. Smowton'.

Prof Peter Smowton
CS Hub Director,
Head of School,
School of Physics &
Astronomy,
Cardiff University

Professor Peter Smowton, CS Hub Director and Head of School of Physics and Astronomy, Cardiff University.

Introduction

EPSRCs vision for their critical mass investments is to support UK manufacturing industries by supporting the commercialisation of early stage research opportunities in emerging areas, through a network of Future Manufacturing Research Hubs.

Each Hub has a programme of innovative research in the engineering and physical sciences, related to the challenges in commercialising early stage research. A key characteristic of the Hub model is that the research is driven by the long-term research challenges of users. User collaboration is therefore an essential aspect for these Hubs.

The vision of The Future Compound Semiconductor Manufacturing Hub (CS Hub) is to establish the UK as the primary global research and manufacturing hub for Compound Semiconductor (CS) Technologies by combining and connecting the UK research excellence in CS, with the very best translational facilities and the new Compound Semiconductor Catapult to support the UK CS industry and UK industry users of CS. The combined activity provides a path from enabling fundamental research through wafer, device and integrated chip manufacturing research into prototyping, reliability testing and system qualification.

The CS Hub has 3 key outcomes :

- To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
- To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
- To generate novel integrated functionality such as sensing, data processing and communication.

The Hub forms an integral part of the CS Cluster based in South Wales, and also serves and

supports CS manufacturing and applications related industry throughout the UK. The CS Cluster forms a complete manufacturing chain from Technology Research Level (TRL) 1 to 9 and currently comprises 9 collaborating partners. The Hub makes use of the world leading facilities and expertise at the Institute for Compound Semiconductors (ICS, Cardiff University) and feeds the higher TRL 4+ activity at the Compound Semiconductor Centre (CSC) which links to the UK manufacturing industry and the Compound Semiconductor Catapult. The Hub is resourced to research and develop new manufacturing processes, leveraging existing capital investment and completing the Welsh and UK Government strategy to generate a major UK CS Cluster.

Compound semiconductors are essential for the development of:

- 5G
- energy efficient lighting
- smart devices
- electric vehicles
- imaging techniques.

Compound semiconductors are vital to development of technologies supporting:

- a connected world
- health
- security
- the environment.

The Hub will:

- position the UK at the centre of CS manufacturing research
- support & promote CS research and systems research in all associated fields
- apply the manufacturing disciplines and approaches used with Silicon semiconductors
- combine CS with Silicon to generate the required increase in CS manufacture.

Introduction



Education Minister Kirsty Williams, Bouygues UK Chief Executive Rob Bradley and Cardiff University Vice-Chancellor Professor Colin Riordan pictured ‘topping out’ the Cardiff University’s Transition Research facility by adding their signatures to a beam on the building’s highest point.



Structure

Internal structures and regulation

Our Hub of CS research activity and operational headquarters is located at Cardiff University, led by Hub Director, Professor Peter Smowton. This central entity interacts highly with spoke including universities: University of Manchester, University of Sheffield and University College London, as well as a large number of industrial partners and collaborators.

The Hub structure includes a Management Board and Strategic Advisory Board, as well as support structures for each of 8 work packages.

Management Board

The Hub Management Board (MB) is responsible for the strategic and operational management of the Hub, including making decisions on the allocation of funding.

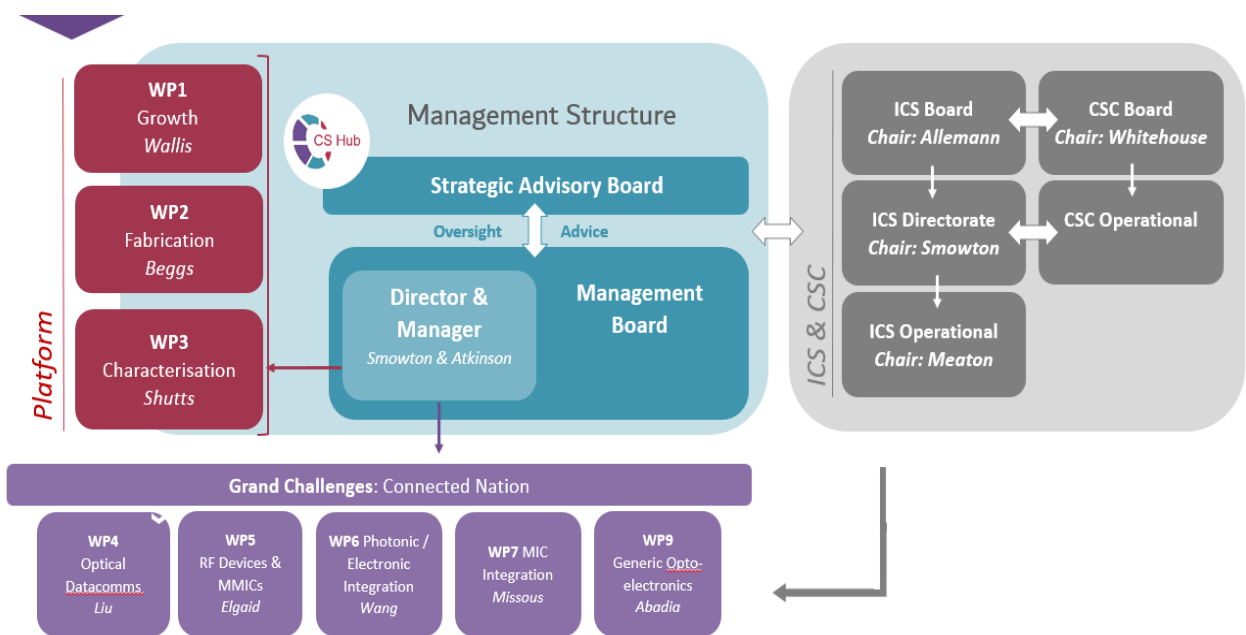
The MB is comprised of a number of senior

Hub members who are able to represent the research interests of the Hub. All members meet quarterly to discuss and plan the research of the CS Hub, in addition to other areas the MB is responsible for, including ED&I and learning and development. The MB reports to the Hub Strategic Advisory Board (SAB) every 6 months.

Strategic Advisory Board

The SAB provide guidance to the Hub MB via a biannual meeting. The Board includes world leading research and industry experts in the field of compound semiconductors.

Strategic Advisory Board meetings provide an opportunity for Hub members to receive guidance and direction from impartial, highly experienced and knowledgeable individuals.



The CS Hub Management Structure. The Director is advised by a Management and Strategic Advisory Board.

Structure

Management Board Members

Name	Organisation
Diana Huffaker	Cardiff University
Peter Smowton	Cardiff University
Paul Tasker	Cardiff University
Wyn Meredith	Compound Semiconductor Centre
Huiyun Liu	University College London
Mo Missous	University of Manchester
Tao Wang	University of Sheffield

Strategic Advisory Board Members

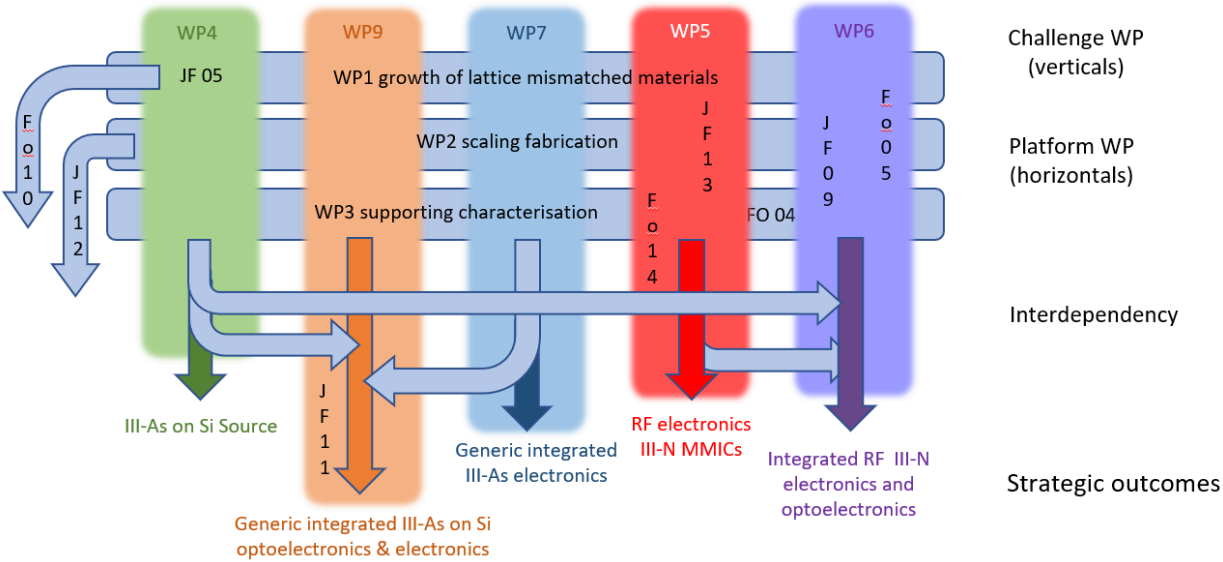
Name	Organisation
Richard Penty	Cambridge University
John Bagshaw	Independent Technology Consultant
Gerald Buller	Heriot-Watt University
Dominique Schreurs	KU Leuven
Andy Sellars	CSA Catapult

Work Package Leads

Name	Organisation	WP Lead
David Wallis	Cardiff University	WP1 Lead
Daryl Beggs	Cardiff University	WP2 Lead
Samuel Shutts	Cardiff University	WP3 Lead
Huiyun Liu	University College London	WP4 Lead
Khaled Elgaid	Cardiff University	WP5 Lead
Tao Wang	University of Sheffield	WP6 Lead
Mo Missous	University of Manchester	WP7 Lead
Nicolas Abadia	Cardiff University	WP9 Lead

Membership of the CS Hub management structures is shown in the tables. The Hub is governed by a Management Board made up of senior members of the Hub team across the four original academic partner institutions. The Strategic Advisory Board is made up of experts from academic and industry who are well equipped to advise the Hub on research direction, identifying commercially valuable research and advising on impact paths. Our work package and grand challenge leads direct and coordinate the research of the Hub.

Structure

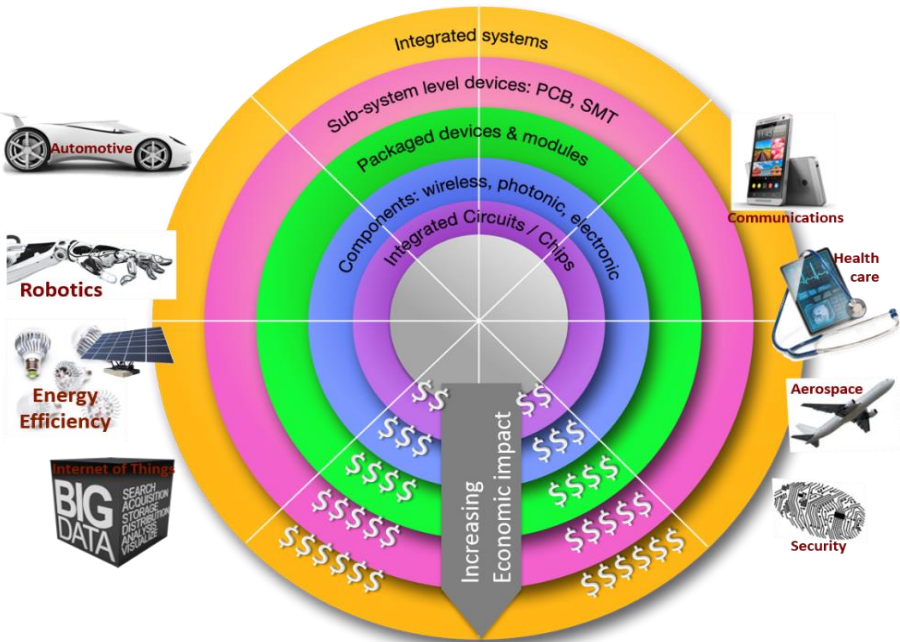


Work Package (WP) structure of the CS Hub. Grand challenge WPs are supported by 3 “platform” areas and have been made more effective by the addition of a number of feasibility (JF) and follow-on (FO) activities from other universities, together focussed on achieving the strategic outcomes.

Next generation technologies will only be achieved with a huge increase in compound semiconductor manufacture.

Compound semiconductor materials are a Key Enabling Technology at the heart of modern society.

- Key Outcomes:
- To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
 - To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
 - To generate novel integrated functionality such as sensing, data processing and communication.



The diagram indicates the likely impact areas of technology developed via the CS Hub and emphasises the added value at each stage enabled by the CS technology.

Research landscape

CS Cluster Developments

The Future CS Hub remains an active and founding member of the CS Cluster in South Wales. CSconnected is now the formal gateway to the cluster which represents organisations directly associated with research, development, innovation and manufacturing of compound semiconductor related technologies, as well as organisations along the supply chains whose products and services are enabled by compound semiconductors.

Other members of CSconnected include core partners, the Institute for Compound Semiconductors (ICS, Cardiff University), the Compound Semiconductor Centre Ltd (CSC), the Compound Semiconductor Applications Catapult and the Centre for Integrative Semiconductor Materials (CISM, Swansea University). These are joined by business partners IQE plc, SPTS, Microsemi (Microchip), and Newport Wafer Fab.

Together we complete the supply chain for bringing new CS discoveries to market. The development of the CSconnected brings us closer to achieving our mission of *“establishing the UK as the primary global CS research and manufacturing hub”*

UKRI Strength in Places

CSconnected received early stage funding from the UKRI Strength in Places Fund for a

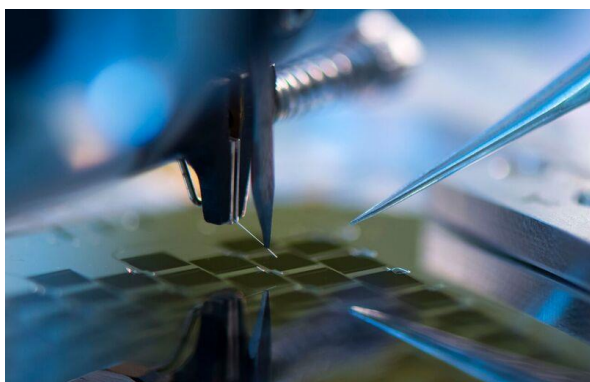
project designed to drive substantial economic growth. Having submitted our full bid, we hope for a successful outcome consolidating CSconnected and bringing significant economic benefit for the South Wales area through high value job creation and regional growth.

CCR City Deal

Significant investment (£38.5m) from the Cardiff Capital Region (CCR) City Deal has enabled cluster members, IQE plc to develop a new high-tech facility in Newport. This has generated employment for a number of highly skilled engineers and technicians.

CS Applications Catapult

In 2018, the CSA Catapult opened an impressive Innovation Centre, which is co-located with IQE in Newport, South Wales. The centre houses a design studio, laboratories and test facilities for power electronics, photonics and RF, supported by simulation and modelling tools and an advanced packaging facility. The Catapult currently employs 80 highly qualified staff, with many educated to PhD level. The Catapult helps companies develop new products using compound semiconductors and is currently working on projects valued at £58m with 20 academic partners and 65 industrial partners.



Research landscape



Image adapted from CS Catapult material. The CS Hub covers TRL levels 1 to 4 and works together with ICS, the CS Centre and the CS Catapult, together with several other partners, to form the CS Cluster.



CSA Catapult Innovation Centre, which is co-located with IQE in Newport, South Wales.

Impact

How will the Hub affect the future of manufacturing research

Societal

Compound Semiconductor materials are a Key Enabling Technology underpinning the operation of the internet and enabling emerging megatrends such as smart phone usage, satellite communications/GPS, direct broadcast TV, energy efficient lighting, efficient solar power generation, advanced healthcare and ground breaking biotechnology. Simply put these technologies support our connected world and the future health of the planet.

Knowledge Dissemination

We are active in dissemination of knowledge via conferences such as UK Semiconductors and Photonics West, the latter providing an excellent mix of science and commercial activity. We will publish in open access peer reviewed journals such as those from both the Nature and IEEE tables.

Our aim throughout is to engage new partners and we will hold workshops, use feasibility funding, actively canvas and make use of our existing partners and contacts, relevant KTNs, the Welsh Optoelectronics Forum and other appropriate bodies to connect as widely as possible.

Skills Base

The cutting edge equipment operated as part of a manufacturing process offers an excellent training opportunity, inculcating a manufacturing mind set in a UK strategically relevant high technology field. We will embed technological excellence and the latest manufacturing approaches in UK industry. PDRAs and students will participate in high level meetings with the commercial organisations and will work alongside R&D staff from industry. There will also be a direct economic impact via the provision of skilled workers to relevant companies.

Outreach

The Hub has recently recruited an outreach specialist who will be coordinating the promotion of compound semiconductors and the outreach strategy and activity of the Hub in manufacturing. The Hub will also increasingly focus on working with schools at different key stages to promote the importance of compound semiconductors and related careers. Researchers from across the Hub will play an active role and use their knowledge to strengthen the Hub's outreach work, as well as further developing their own communication skills.

Economic

Our vision is to ensure that the UK's research strength in compound semiconductors will be embedded in manufacturable approaches so the UK can commercially address the opportunities that compound semiconductors will provide. The global market for compound semiconductors is currently worth over USD 37bn and is expected to grow to 50 billion USD by 2024; with growth predicted to be between 5 and 7% over the next 4 years. It underpins 100s of billions dollar related industries from telecom to automotive. Expanding commercial activity in the compound semiconductor sector will provide an important boost for the UK economy and maintain UK advanced manufacturing competitiveness. A good example of this is Cardiff headquartered IQE Plc, the global leader in supplying compound semiconductor materials (156 turnover, 2018 results).

Our aim is to strengthen the relationship between academia and industry and this will be achieved by 1) changing the mind set of researchers to start from solutions that allow rapid translation to production by providing access to production scale and research tools that are functionally similar along with highly skilled support for the tools and processes; 2) Co-location of research and industry staff to maximise cross fertilisation of ideas, techniques and approach in an environment that supports interaction.

The Hub together with staff from the Compound Semiconductor Centre will support SMEs through product prototyping, IP generation, skills development and training. They will help bid for external grants, coordinate partner forums, form networks and prepare roadmaps.

Translation

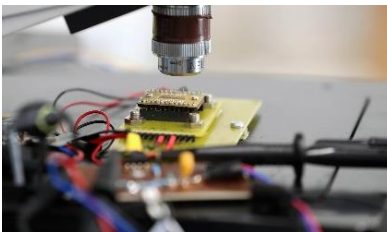
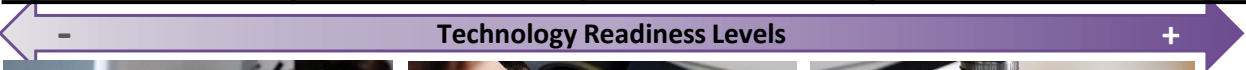
Industry / user / Innovation chain engagement

In 2014 the Sheffield led EPSRC III-V centre CS roadmap identified a concern that the UK CS community was missing an exploitation link to help provide a route to impact and exploitation. Many technological solutions work well in the research environment but fail to succeed commercially. The Hub directly addresses this issue, by working to change the academic community mind set, to inspire researchers, via training and environmental changes, so they begin with solutions that allow rapid translation.

The Hub is encouraging the co-location of research and industry staff to maximise interactions. Our research is specifically designed to produce intermediate outputs that can be used to demonstrate the potential for successful translation.

CS Connected: User interface, represents cluster members including those below.

Future Compound Semiconductor Manufacturing Hub	Institute for Compound Semiconductors	Compound Semiconductor Centre	Compound Semiconductor Applications Catapult
CS Manufacturing Research	Facilities; Equipment; Services (skilled workers)	Develop and prototype CS materials	Accelerate the development of products using compound semiconductors
Enable high value & productivity in CS manufacturing	Research	Enable a wide range of applications	Market intelligence Consortia building Supply chain management Project management
Building on CS research	Product development to prototyping	Transfer R&D to product & process innovation to high value large scale manufacturing	Design studio with simulation and modelling Power electronics lab Photonics lab RF/microwave lab Advanced packaging lab
Training; Outreach	Industrial collaboration		Knowledge Transfer Partnerships



Images show device development by a Hub PhD student, Cardiff University.

Comments from industry partners

Mohsin Haji, Senior Research Scientist working in the Quantum Metrology Institute at the National Physical Laboratory

“The CS Hub offers pioneering capabilities in developing highly advanced laser diodes for a wide range of quantum applications, including enhanced atomic clocks, magnetometers, gravimeters and quantum computers. Equipped with world-class infrastructure and resources geared towards performing efficient research, design and manufacturing of laser diode prototypes that are primed for scaling up to high volume production at the same facilities, the CS hub are an integral part of the supply chain for several new state-of-the-art quantum systems and products emerging from the NPL QMI.”

Dr Andy G Sellars, Strategic Development Director, CSA Catapult

“The EPSRC Future Compound Semiconductor Manufacturing Hub, hosted at Cardiff University, has made a strong impression since it was established in 2016. The Hub is working on an interesting number of projects that are aligned to the needs of industry in the near term, and other projects that have longer term goals – providing a degree of resilience to the Hub’s activities.

There is good evidence the Hub is capitalising on the combined expertise from Cardiff University, Manchester University, Sheffield University and University College London. In addition, the Hub has made excellent routes to commercialisation by working with industrial partners in the compound semiconductor cluster, such as Newport wafer Fab, and other research institutes, such as the Catapult. The Hub has shown demonstrative market pull working with large industrial companies from across the UK.

Some projects are particularly impressive, spanning the research spectrum from cutting edge ideas to market acceptance, and spanning the supply chain from semiconductor materials to sub-systems. Of particular note, the advanced quantum well hall effect sensor project spun-out of Manchester University shows great market potential.”

Expertise at the Hub

The CS Hub investigators and associated groups have been carefully selected for their track record in innovation and impact, complementary technical capability and the individual skill sets that can combine to create new solutions to the identified major scientific challenges in manufacturing.

Expertise in epitaxial growth, including growth on non-native substrates is provided by Huffaker, Li, Liu, Missous, Wallis, Wang and Wu. Buckle, Elgaïd and Missous bring experience of wafer scale-up and manufacturing uniformity over these larger wafer sizes. Abadia, Beggs, Quaglia, Smowton and Tasker bring world leading expertise in design, integration and characterisation.

In addition to the Hub's Work Package Leads, we work with a number of world-leading academics to develop the highest impact research possible under the remit of the Hub.

Diana Huffaker (Cardiff University) (h-index 47) is the Welsh Government Ser Cymru Chair in Advanced Materials and Engineering and is a Director of ICS. She has made major contributions in compound semiconductor material and devices and, of particular relevance, in the growth of Compound Semiconductors on mismatched substrates including Silicon. Her current research

interests include the directed and self-assembled nanostructure solid state epitaxy and optoelectronic devices including infrared detector arrays, solar cells and III-V/ Si photonics.

Michael Pepper FRS, FEng (UCL) (h-index 55, 8 patents) is Pender Professor of Nanoelectronics and has received the Royal Society's Bakerian Prize Lectureship, Hughes and Royal Medals. He is co-founder and Scientific Director of THz technology spin-off company TeraView. He is a former member of General Board and Council of Cambridge University and Council for Industry and Higher Education.

Alwyn Seeds FEng, FIEEE (UCL) is Professor of Optoelectronics. He pioneered the research area of microwave photonics and was awarded the Gabor Medal and Prize of the Institute of Physics in 2012. He is an inventor on 16 patents and is co-founder of Zinwave Ltd, which is now the third largest supplier of wireless over fibre systems in the world and was acquired by McWane Technologies Inc. in 2014.

These staff are supported by academics Rick Smith & EPSRC Manufacturing Fellow Jon Willmott (Sheffield), Max Migliorato (Manchester), and Senior Research Fellows Siming Chen (UCL) and Sang Soon Oh (Cardiff) covering design, nitride fabrication, and characterisation and growth of CS on Si.

Wafer loading onto ellipsometer in the Institute for Compound Semiconductors (ICS) clean room, Cardiff University. The ellipsometer was purchased using the CS Hub underpinning equipment award from EPSRC.



New expertise at the Hub

Evolving the expertise available at the Hub

The Hub has worked flexibly to ensure that our research remains highly relevant in the constantly evolving CS manufacturing environment. We have welcomed several new people to the team during year 3, bringing with them a variety of expertise essential to keep the Hub at the very peak of research excellence.

Dr Samuel Shutts has taken over leadership of Work Package 3 (Fast Fabrication and Characterisation) from Prof Peter Smowton. Sam brings expertise in characterisation and fabrication of lasers and VCSELs. His management of the Work Package is a good example of progression within the Hub.

This progression has also been mirrored by Dr Daryl Beggs taking over leadership of Work Package 2 (Fabrication) from Khaled Elgaid. Daryl brings expertise in design, layout and fabrication.

The Cardiff lab team have also been joined by a new post-doctoral research associate, Harry Gordon-Moys and Grace Mullally joins the team at Cardiff University in an outreach role.

New CS Hub associated PhD students in Cardiff include Jack Baker, who has joined us as an IQE sponsored student and is working on VCSELs; Joe Mahoney working on generic photonics. Maryam Alsayyadi working on InAs quantum dot lasers; and Nourh Almalki working on nano wire devices.

Other new CS Hub associated PhD students working across the Hub include Guillem Martinez de Arriba (Sheffield), working on on the optical characterisation of micro-LED array devices.

Ruslan Murshudov (Manchester), working on Non-destructive flaw detection and profiling in paramagnetic materials using QWHE sensors; Alex Lindley (Manchester), working on "2D Arrays of Quantum Well Hall Effect Sensors for Picotesla Magnometry of Inorganic and Organic Materials".



Dr Samuel Shutts
the new Work
Package 3 lead
(Fast fabrication
and
characterisation),
Cardiff
University.



Grace Mullally,
Outreach
Officer, Cardiff
University



Dr Daryl Beggs
the new Work
Package 2 lead
(Fabrication),
Cardiff University

Equality, Diversity and Inclusion

An inclusive environment and culture

Over the past year, we have sought to further embed an inclusive culture and environment for staff and students working across the Hub; building on the policies and existing good practice that exists across each of our partner institutions.

To help achieve this, the Hub has developed an expanded Equality, Diversity and Inclusion (ED&I) plan which sets out our priorities, including: creating a supportive culture which helps to underpin the protected characteristics; achieving greater diversity within the Hub; taking further steps to directly address unconscious bias; and improving diversity amongst our staff, management and advisory boards.

One of the ways these priorities have been addressed over the last year is through the development and delivery of unconscious bias training to further develop staff knowledge and understanding in this area.

The protected characteristics under Equality Law are:

Age

This refers to a person belonging to a particular age or range of ages (e.g. 18 - 30 year old). The law says you shouldn't treat someone/people badly for reasons relating to their age (whether young or old).



Disability

A person has a disability if s/he has a physical (including serious illness) or mental impairment that is likely to last a long time (a year or longer) and makes their normal day-to-day activities much more difficult.



An extract from the Hub unconscious bias training materials.



The interactive training session allowed participants to explore protected characteristics in greater detail. Attended by researchers and PhD students from across the Hub, the face to face session was tailored to the specific experience of the research environment staff work in across the Hub.

Staff built their awareness of unconscious bias through a series of activities and group discussions which enabled them to openly and honestly share their experiences, as well as exploring areas such as micro inequalities and the culture and values of the Hub. The training also looked at different approaches to addressing unconscious bias and how these might be practically applied to the research environment.

The knowledge and skills developed during the training built upon those which staff have developed through the completion of online unconscious bias modules and explored their practical application; as well as communicating to staff that this is one of the Hub's ED&I priorities. In the year ahead we will run wider ED&I training for staff across the Hub, as part of an expanded learning and development programme with ED&I at its core.

Platform work package 1

Materials Growth (Epitaxy)

Summary

This work package is addressing the key challenge of growing high quality compound semiconductor layers. In many cases this involves growth on to substrates with large lattice mismatches. A particular focus is the growth on to Si substrates to allow, low cost, large volume manufacturing of the devices being developed with in the Manufacturing Hub.

Lead: Prof. David Wallis

Email: WallisD1@Cardiff.ac.uk

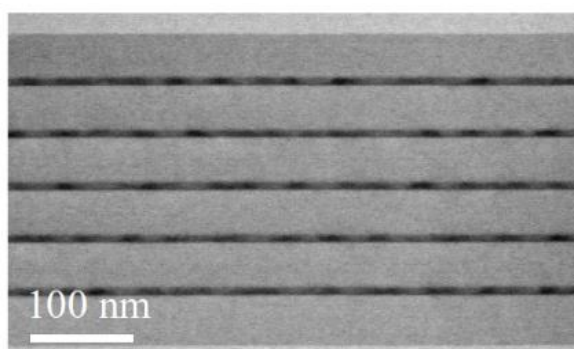
Contributing academics: include Tao Wang (Sheffield), Mo Missous (Manchester), Huiyun Liu (UCL), and Qiang Li (Cardiff). We also have a project partner, Manus Haynes, who is working on a Future CS Hub sponsored feasibility study: "Feasibility of compound semiconductor non-volatile RAM manufacturing on Si substrates".

WP1 encompasses all the epitaxy activities that are relevant to the CS Hub. These include non- and semi-polar GaN growth for optoelectronics, III-As for photonic integration, metamorphic structures on GaAs for magnetic sensors and arsenides and phosphides for optical devices.

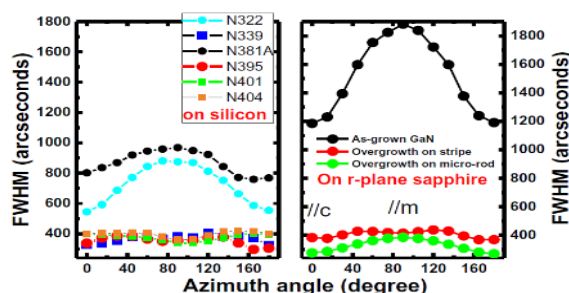
Progress and challenges

In the last year some significant improvements have been made to the capabilities of the hub partners. In Cardiff, a new MOCVD system for growth of Arsenides, Phosphides and Antimonides has come on line and has demonstrated growth of all 3 of these materials systems. Basic device structures have been developed and now work is focussed on transferring these on to Si substrates. At UCL funding has been won to install a new MBE tool that will be dedicated to the growth of only Arsenide structures. This will enable layers with much lower background impurities to be achieved. The new system has been installed in the UCL MBE lab and is currently being commissioned

In terms of project deliverables, deliverables, many of those defined at the start of the Hub have now been successfully completed. These include, growth of non-polar GaN layers on Si with record XRD FWHM values, growth of metamorphic Phosphide based HEMT structures with world leading carrier concentration and mobility and Quantum dot laser structures with record high temperature operation. Moving forward we have defined a new set of deliverables which focus on some of the manufacturability issues associated with the technologies being developed. These will address issues such as the control of interface strain in GaAs on Si structures, development of patterned structures to control strain and wafer bow in non- and semi-polar GaN on Si layers and studies of the impact of strain on the processability and yield in metamorphic HEMT structures.



TEM image of an InAs/GaAs Q-dot laser structure with a maximum operating temperature of 126°C grown on a Si substrate.



X-ray FWHM data for non-polar GaN grown on Si (left) and sapphire (right) substrates. The FWHM values for these layers are amongst the best reported internationally.

Platform work package 2

Autoprober Capability and Application to 150mm Wafer Scale Passive Components

Summary

As activities within the hub are scaled up from research towards manufacturing several 100s of devices, the ability to rapidly characterise becomes essential. In commercial production, routine monitoring at various stages is undertaken to keep fabrication processes within specification/yield by collecting cross-wafer statistics, ensuring product quality.

Lead Academic: Dr. Daryl Beggs

Email : Beggsd@Cardiff.ac.uk

With thanks to David Hayes

WP2 is about developing reliable and reproducible fabrication processes and particularly these processes at scale. However, fabrication cannot be considered in isolation and to complete WP2 it is essential to be able to test large numbers of fabricated devices, components and circuits across large format wafers e.g. 150mm or 200mm diameter.

Our industry standard automatic wafer prober can do that and more. Coupled with high frequency and optical test equipment it delivers a powerful research tool that is reconfigurable to combine dc, ac (to 125 GHz) and optical probe measurements which are tailored specifically for each device type, over wafer diameters up to 200mm. An example of electro-optical testing is shown in Figure 1.

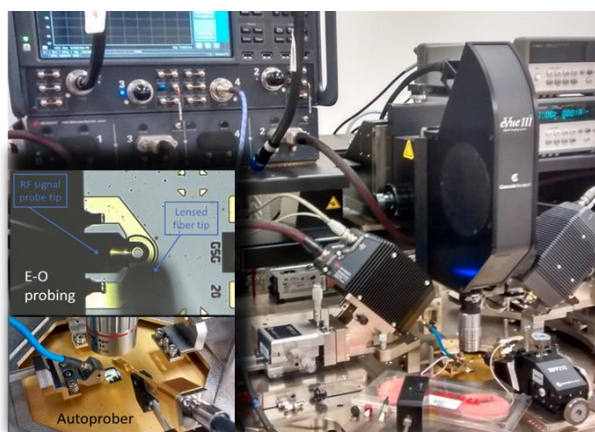


Figure 1 Electro-optical modulation bandwidth testing on a VCSEL.

Progress and challenges

Passive capacitor, inductor and resistor components are necessary to e.g. realise GaN monolithic microwave integrated circuits (MMICs) of WP5 and the on-chip circuits integrated with the detector arrays of WP7. Scaling-up of the passive fabrication processes is initially carried out on GaAs wafers. Measured results for passives fabricated on and across 150mm diameter GaAs wafers are presented in Figure 2, where dc continuity of the spiral inductors and dc leakage of the dielectric capacitors is pass/fail mapped. The maps clearly illustrate high failure regions, which are subsequently investigated in more detail to flag up inappropriate fabrication approaches and improve fabrication procedures and process steps.

Automatic probing at the wafer level reduces cost and speeds up development of material and process characterisation, and mm-wave/photonic integrated circuits.

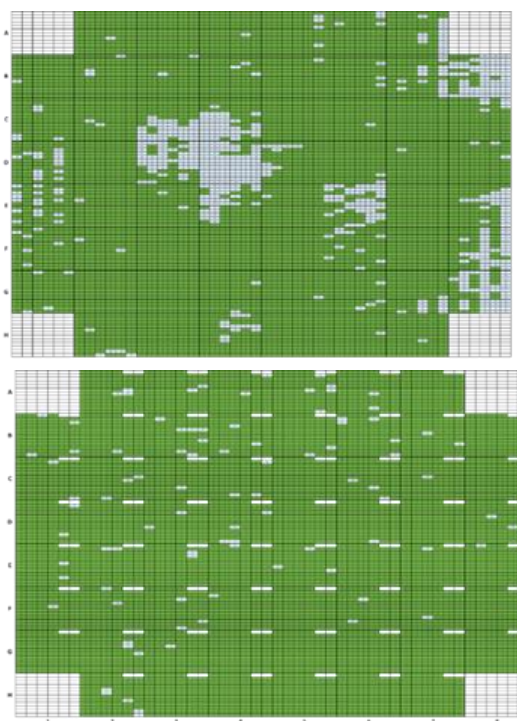


Figure 2 Top: Map of dc continuity on 4,320 inductors. Bottom: Map of dc leakage on 4,320 capacitors. In both maps green = pass; light blue = fail and white = no device present.

Platform work package 3

Fast Fab and Characterisation

Summary

Recent technical and scientific challenges have involved: fast-fab of vertical cavity surface emitting lasers (VCSELs); scaling up characterisation for optical devices using auto-probe wafer-mapping; reporting degradation mechanisms of III-V lasers on Si, testing and expanding existing device degradation studies and developing fabrication and measurement techniques for mode-locked lasers.

Lead Name: Dr Samuel Shutts

Email: ShuttsS@Cardiff.ac.uk

Contributing academics: N. Abadia, D. Beggs, K. Elgaid, H. Liu, M. Missous, R. Quaglia, R. Smith, P.M. Smowton.

To develop fast fabrication and characterisation techniques to feedback to design and growth, minimising development cycle time. The key work package deliverables include, reliability measurements (III-Vs on Silicon), fast-fab on large area VCSEL wafers, in-line characterisation to support integration.

Progress and challenges

Using a newly installed Bentham monochromator we have upgraded our capability to for fast characterisation of VCSEL epi wafers, via photovoltage spectroscopy. The technique, which is a much faster than fabricating and testing VCSELs, allows the QW transition energies to be determined and the cavity resonance, which will define the VCSEL lasing wavelength. This is valuable information which can be fed back to design and production teams, to inform wafer spec and determine if growth parameters need to be adjusted.

The auto-prober (Figure 1) has been used extensively to develop a fast turnaround VCSEL fabrication and characterisation process in order to rapidly assess different VCSEL designs. This work is a collaboration between wafer supplier (IQE), processing facility (ICS) and CS Hub WP3. Real measured results are presented in Figure 2, where the ON-resistance of 900 VCSELs are displayed as a heatmap, and example light-current-voltage (L-I-V) characteristics and spectra at shown for two VCSEL sizes. Automatic probing at the wafer level reduces cost and speeds up development of material and process characterisation.



Figure 1. Electro-optical probing on a VCSEL tile.

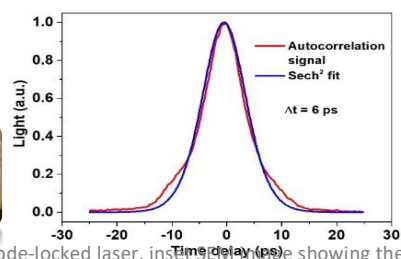
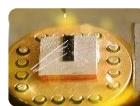
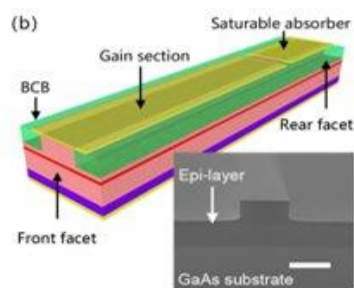


Figure 3: Monolithic integrated two-section passive mode-locked laser, inset showing the cross-section profile, the scale bar is 2 μm (left); bonded laser (middle); Autocorrelation trace from an InP QD mode-locked laser. (right).

We have reported on the degradation mechanism for III-V QD lasers directly grown on Si substrates, which appears in IEEE Journal of Selected Topics in Quantum Electronics (Volume: 25, Issue: 6, Nov.-Dec. 2019). We have upgraded the reliability and degradation study facilities to achieve semi-automated testing. First experiments on 1.3 μm emitting InAs QD lasers were successfully completed in Q4 2019, with a run time of 1076 hours. These lasers were developed as part of WP4 and we are working towards longer term studies, at further elevated temperatures in 2020. To support WP9, we and subjected them to harsh radiation environments in collaboration with our industrial partners. The aim is to simulate environments that will be experienced in the applications targeted in WP9. Initial results show excellent promise and further radiation experiments are planned for 2020.

We have developed a fabrication process for monolithic passively mode-locked lasers utilising indium phosphide (InP) quantum dots (QDs) emitting in the 730nm waveband. Researchers at the CS Hub, in collaboration with colleagues at Heriot-Watt University have characterised the passive mode-locking properties of these devices with pulse widths of 6ps, at a repetition frequency of 12.55 GHz having been measured. Full details of this work have been submitted for publication, with the manuscript currently under peer review.

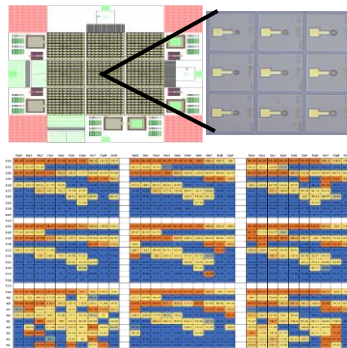
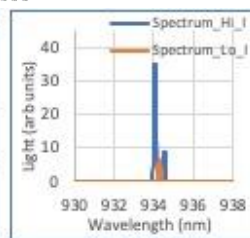
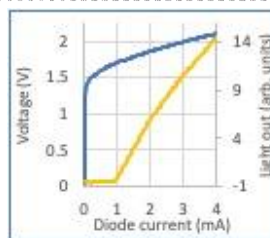


Figure 2: Fast-fab VCSEL tile layout and expanded microscope image of VCSEL array (top left); Map of ON resistance for 900 VCSELs (bottom left). L-I-V & spectra (at two currents) for a single VCSEL (right).



Work package 4

Manufacturing Technology for Optical Data Communications on Silicon

Summary

Recently, high-performance silicon-based InAs/GaAs quantum dot (QD) lasers have been demonstrated with CW operation at high temperature ($>75\text{ }^{\circ}\text{C}$) and long lifetimes ($>100,000$ hours) by UCL and Cardiff. Here we will further develop our world leading III-V-on-Si technologies to create high performance lasers and semiconductor optical amplifiers (SOAs) for datacommunications applications.

Lead Name: Prof. Huiyun Liu

Email: huiyun.liu@ucl.ac.uk

Contributing academics: Prof. Peter Smowton, Prof. Alwyn Seeds, Dr Qiang Li, Dr Siming Chen, Dr Sam Shutts

The principal objectives are to optimise gain per unit length (for high frequency) and to increase operation temperature to the required $>125\text{ }^{\circ}\text{C}$, while maintaining low current CW operation at 20 mW optical output power. This will be achieved by exploiting p-type modulation doping in lasers and optimizing/combining nucleation layer, dislocation filter layer as well as thermal annealing. To increase the gain of the QD active region, P-type modulation doping and high QD density are investigated in last 18 months and initial results are very promising.

Progress and challenges

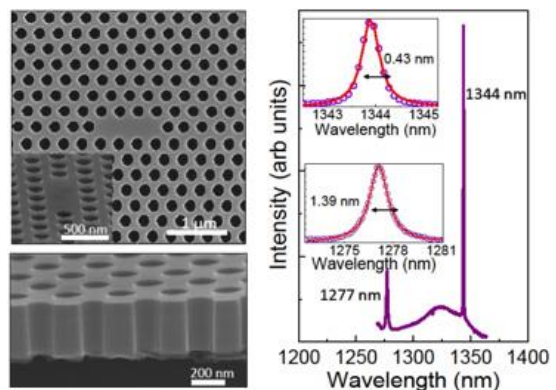
High-performance InAs/GaAs QD devices have been demonstrated by growing on high-quality GaAs/Si virtual substrates developed by exploiting new epitaxial growth technologies and new epitaxial structures in this WP. The detailed achievements are as following:

The silicon-based GaAs buffer layer with defect density $<10^6/\text{cm}^2$ was successfully demonstrated by utilising InGaAs/GaAs superlattice layers and novel III-V nucleation layers on Si and Ge epi surface. Lasing up to $130\text{ }^{\circ}\text{C}$ has been demonstrated for InAs/GaAs QD lasers grown on this high-quality GaAs buffer on silicon substrates. To the best of our knowledge, this lasing operation temperature ($130\text{ }^{\circ}\text{C}$) is the highest operating temperature for lasers monolithically grown on silicon. To increase the gain of QD lasers, high-density QD growth and p-type modulation doping have been studying in last 18 months. The high InAs/GaAs QD density of $>5.0 \times 10^{10}\text{ cm}^{-2}$ was delivered for the purpose of the Hub. At the same time, p-type modulation was extensively investigated by different designs. The InAs/GaAs

QD lasers with very short cavity of 0.333 mm was achieved with the best design so far. The expertise on the design of p-type modulation doping for high-gain QD laser devices, developed in this WP, is internationally leading.

The antiphase-boundary-free III-V growth on complementary metal-oxide-semiconductor (CMOS) compatible on-axis silicon (100) substrate is very important for the monolithic integration of III-V photonic materials and devices with the mature CMOS technology. The growth of III-V buffer on on-axis silicon (100) substrates by MBE is developed by using UCL twin MBE system, in which group-IV MBE growth chamber are connected with III-V growth chamber by an ultra-high-vacuum buffer chamber. The growth of Si epilayer is critical to annihilate antiphase boundaries for GaAs growth on silicon substrates, and the mechanism behind it is explained for first time. These results are proof of concepts and internationally leading.

Semiconductor Nano-Laser is very important for the next generation of Si-based on-chip optical interconnects. III-V photonic crystal (PC) laser is regarded as a promising ultra-compact light source with unique advantages of ultralow energy consumption and small footprint. Very recently, the first QD Photonic Crystal laser grown on silicon has been demonstrated as proof of concepts for Nano-Lasers on Si. This work establishes a new route to form the basis of future monolithic light sources for high-density optical interconnects in large-scale silicon electronic and photonic integrated circuits. This result is world lead and was published at Nature Communications 11, 977 (2020).



A InAs quantum dot photonic crystal cavity laser monolithically grown on on-axis Si substrate (001). Top-view and tilted cross-section view SEM images of the fabricated PC cavity. The laser spectrum shows the ground state emission at 1344 nm and excited state emission at 1277 nm, which has narrow linewidth of 0.43 nm and 1.39 nm, respectively.

Work package 5

Advanced Radio Frequency Devices & MMICs

Summary

Building on on-going success, the aim of this work package is to demonstrate a UK III-V-on-Si GaN based HFET technology baseline. Specifically targeting wireless applications, this work package aims to ultimately establish a full III-V-on-Si HFET device, a collection of passive devices and a MMIC technology platform suitable for high to medium power microwave 5G system applications. This work package uses high-frequency device characterisation at staged points to allow feedback for the optimisation of the epitaxial growth to reach device performance and a fully integrated on-chip technology in line with industrial requirements. This work package activities are closely aligned with major compound semiconductor manufacturing industry partners including Newport Wafer Fab (NWF), IQE, SPTS and the CSA Catapult.

Lead Name: Prof. Khaled Elgaid

Email: ElgaidK@Cardiff.ac.uk

Contributing academics: Prof. Paul Tasker & Dr. Roberto Quaglia

The WP5 focus is to develop advanced GaN on Si RF active and passive devices and implement them through the realisation of high-performance MMICs operating at X-band and Ka-band. The technology development in this WP interacts with other work packages in the CS Manufacturing Hub and strongly links with several key industry partners in areas of both technology and design; NWF, SPTS, IQE, MBDA, NTT, Toshiba, CSA Catapult, Leonardo, Huawei Europe and IconicRF.

Progress and challenges

Typical GaN HFETs for these applications are fabricated on SiC substrates, which are unfortunately limited in size (<150mm) tend to be very expensive. An alternative solution is to use Si substrates, since these can be very large (>300mm) and low-cost. To date, the RF performance of GaN HFETs fabricated on Si is poor in comparison to those fabricated on SiC, due mainly to large lattice mismatch as well as relatively poor thermal conductivity. In addition, the conductivity of Si substrates is not compatible with the realization of low-loss passive matching structures needed in MMIC based technology.

Irrespective of the substrate used, for high speed/frequency electronic devices and circuits there is the need for short gate lengths (L_g) Increase intrinsic transistor performance; hence the

requirement of e-beam lithography-based 0.25 μ m) and small source/drain gap ($\leq 4\mu$ m) to technology. Ensuring a corresponding increase in extrinsic performance requires the appropriate scaling of device parasitics and dimensions; for example, a high gate-to-channel aspect ratio must be maintained. This requires optimization of the epitaxial layer structure and growth. Device layout optimization to minimize capacitive and inductive loading is undertaken using EM-modelling supported by RF characterization. Minimization of access resistances requires very low contact resistance, and to address thus, processes such as epitaxial re-growth are being considered. A staged approached transitioning from unit-cell RF HFET devices, thru RF HFET power-bar structures and passive components, to a full HFET MMIC process is envisaged. At each stage, an appropriate Process Development Kit (PDK), allowing the simulation and design of active circuits, will be developed and supplied to end-user industrial partners for evaluation and feedback. This will start with 100mm and move to 200mm Si substrates.

Advanced RF devices & MMIC technology realisation has so far been progressed by developing several fabrication modules taking into account the requirements for a full integrated on-chip circuits. This includes active device technology optimisation, epi layer design enhancement and low-loss integrated passive device design and development.

Initial activity at Cardiff has focused mainly on defining and acquiring the necessary tool-set for both optical and e-beam fabrication of HFET devices. A detailed plan involving the coordination of all RF processing projects, under the leadership of Prof. Khaled Elgaid, has been implemented with the objective of ensuring that deliverables associated with the development of unit-cell RF devices and RF power-bars can be achieved. This has resulted in the initial GaN on Si active and passive devices development at Cardiff University and the research team at the Centre of High Frequency Engineering (CHFE) are now in the process of fabricating completed designed MMICs and novel high-performance passive devices for on-chip integration.

Characterisation capability within the Centre of High Frequency Engineering at Cardiff University has been upgraded to allow for on-wafer electrical - electrical measurements up to 130GHz; ensuring the ability of full small-signal characterization of a device, as well as of its high-power nonlinear behaviour.

Work package 6

Monolithic Integration of RGB LEDs & Integrated RF Electronics for LiFi

Summary

Building on the work in the platform our approach is to integrate nitrides micro light emitting diodes (μ LEDs) and HEMTs on a single wafer in order to demonstrate and then manufacture monolithic on-chip integration of μ -LEDs and HEMTs for ultra-high resolution & ultra-high efficient micro-displays and ultra-fast & zero cross-talk for Li-Fi; We will continuously develop industrial compatible epitaxial overgrowth steps to integrate CS/Si structures with different designs on the same substrate.

Lead: Prof. Tao Wang

Email: t.wang@Sheffield.ac.uk

Contributing academics: Prof. Huiyun Liu, Prof. Alwyn Seeds, Dr. Rick Smith, Prof. Peter Smowton, Prof. Khaled Elgaid

Li-Fi exhibits striking advantages compared with current Wi-Fi technology in terms of bandwidth, data transmission speed. The major component of Li-Fi is visible LEDs which need to have ultra-fast response time and need to be controlled by high frequency electronic components. The most promising approach to achieving high bandwidth and high data transmission rate for Li-Fi to utilise μ -LEDs. Furthermore, AR & VR micro-displays, smart watches and smart phones require μ LEDs with an ultra-small dimension, high EQE and narrow spectral linewidth. On-chip epitaxial integration of III-nitrides μ -LEDs and HEMTs on low cost and up-scalable silicon substrates for Li-Fi and micro displays is the best way forward, where the LEDs transmitters can be controlled by GaN based HEMTs uniquely.

We aim (1) to develop a disruptive technology for manufacturing monolithic on-chip epitaxial integration of CS electronics and optoelectronics; (2) to demonstrate and then manufacture monolithic on-chip integration of μ LEDs/HEMTs with the highest Max. EQE of >20% for micro-displays; (3) to demonstrate and then manufacture monolithic on-chip integration of μ -LEDs, HEMTs, Waveguides, Photodetectors for Li-Fi (> 20% Max. EQE and >2 GHz modulation

bandwidth); (4) to demonstrate and then manufacture monolithic on-chip integration of μ -LEDs with DBRs and HEMTs for ultra-high resolution & ultra-high efficient micro-display (a pixel diameter of $\leq 5 \mu\text{m}$ and an inter-pitch of $\leq 2 \mu\text{m}$) and ultra-fast (>2 GHz) & zero cross-talk for Li-Fi; (5) to establish and then develop a spinout into a global manufacturer of monolithic on-chip integration systems;

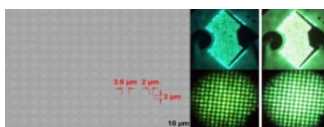
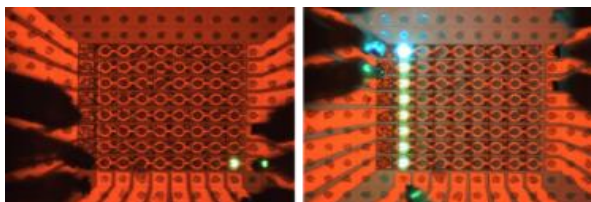
major challenges:

(1) the development of compatible flip-chip processes for monolithic on-chip integration; (2) Further strain engineering by using an extra mediate layer; (3) a combination of MOVPE and MBE to integrate III-nitrides with GaAsP (AlGaAsP) on patterned substrates

Progress and achievements:

(1) Developed a patented approach to on-chip epitaxial integration of μ LED arrays; (2) Demonstrated ultra-small and ultra-compact μ LED arrays with a record EQE and the narrowest spectral linewidth (μ LEDs with $3.6 \mu\text{m}$ in diameter, $2 \mu\text{m}$ in inter-pitch and 9.5 % Max. EQE); (3) Demonstrated 1st monolithic on-chip epitaxial integration of μ -LEDs/HEMTs with a record modulation bandwidth of >1 GHz; (4) Demonstrated GaN HEMTs with a record highest breakdown field (2.5MV/cm), extremely low leakage current (100 nA/mm) and excellent Figure of Merit $5.13 \times 10^8 \text{ V}^2/\Omega\cdot\text{cm}^2$; (5) Developed a patent approach to achieving a non-polar GaN photodetector exhibiting exhibits a record high responsivity which is 4 orders of magnitude higher compared with the current state-of-the-art, and a record fast response time which is three orders of magnitude faster than the current state-of-the-art; So far, WP-6 has led to (1) 3 plenary talks, 6 invited talks, 32 journal papers and 42 conference papers; (2) 4 IP Patents; (3) the organisation of the 3rd Industrial Event, attracting >15 industrial companies.

As a result of the innovation of from WP-6, EpiPix, the Sheffield's spin-out dedicating epitaxial integration of μ -LEDs/HEMTs, has been officially founded on 20th Jan 2020, currently finalizing £10M investment;



EpiPix

Work package 7

Magnetic Arrays

Summary

The approach is the integration of high electron mobility, high magnetic sensitivity 2DEG structures with on board analogue and digital electronics to deliver scanning magnetic imaging systems for Non Destructive Testing of metallic and composite materials

Lead: Prof M.Missous

Email: m.missous@Manchester.ac.uk

Contributing academics: Dr M. Migliorato and Dr P. Buckle

The overarching theme of WP7 is magnetic imaging of ferrous and non-ferrous materials. The work follows a vertically integrated approach starting from epitaxial growth of advanced 2DEG structures with tailored magnetic sensitivities to device fabrication of integrated arrays and passives, packaging and finally system integration for imaging of flaws, defects and microstructures (See Figure 1 below).

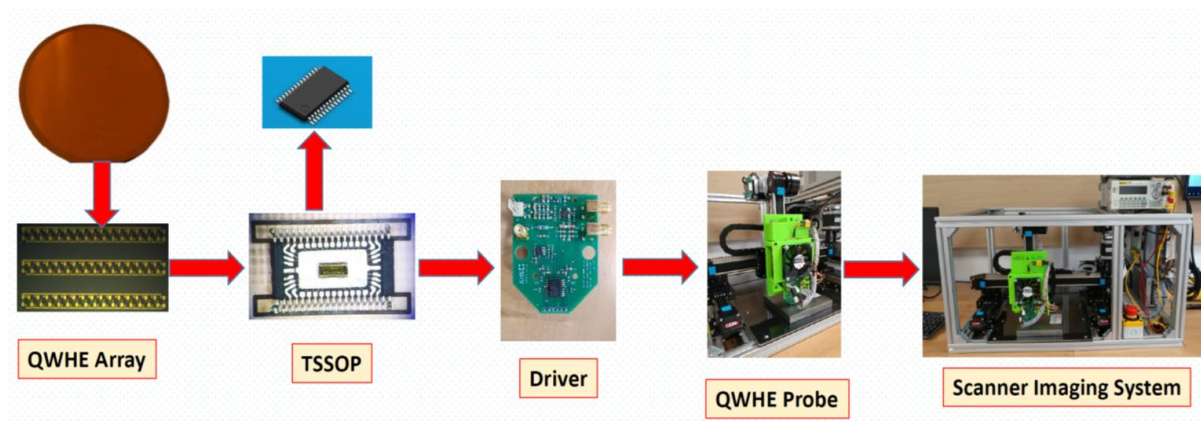


Figure 1 Vertical integration of magnetic imaging of defects, flaws and microstructures

Progress and challenges

During the period magnetic imaging modality using Quantum Well Hall Effect sensors (QWHE) for both ferrous and non-ferrous materials were developed. The work to date has led to ~ 10 journal publications and 24 conference presentations spanning from epitaxial growth to full system demonstrations with key challenges being imaging and classifications of flaws and defects in metals.

Impact has been very strong Impact as demonstrated in 6, separate, fully funded collaborative

INNOVATEUK projects with [Renishaw, TWI, EtherNDT, FarUk, Wright, Home office, BAESystems] in imaging micron size flaws in high value steel to decimeter concealed threats (knives and guns) as shown in Figure 2 below

The work to date in WP7 has concentrated on both ferromagnetic (and non-ferromagnetic) materials mainly using flux leakage as the means to detects flaws and microstructures using low frequency (below 10kHz) illumination techniques. We have now started looking at composite materials using conductivity as the imaging modality which has necessitated the use of very high frequency (MHz) interrogation techniques. The high frequency techniques also result in much more compact imaging systems that are ideal for aerospace applications.

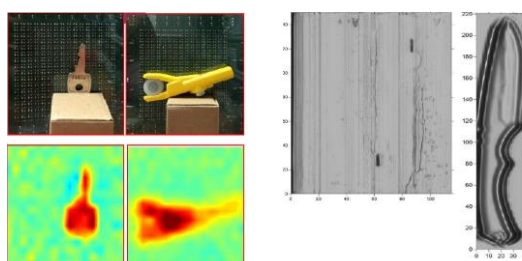


Figure 2(a) metallic imaging and (b) micron size flaws in high value steel and concealed threats (guns).

Work package 9

Generic Photonic Integration:

Summary

Work Package 9 comprises of generic photonic integration work on proof-of-concept optoelectronic devices and systems. The short-term driver for this technology is the provision of GaAs-based integrated optoelectronic devices and systems for interconnects used in aerospace and nuclear sectors and ultimately for telecommunication networks in the long-term.

Lead: Dr Nicolás Abadía

Email : abadian@cardiff.ac.uk

Academic partners: Prof. Huiyun Liu, Prof. Dame Xiang Jane Jiang, Dr Haydn Martin, Prof. Tao Wang.

Generic Photonic Integration is a platform that allows the production of photonic integrated circuits (PIC). PICs are similar to the electronic integrated circuits used in computers and other electronic devices. The main difference between the photonic integrated circuit and the electronic integrated circuit is that the former works with light and the latter works with electricity.

The invention of the integrated electronic circuit was in the United States in 1958 and revolutionized electronics and our daily lives. The field progressed very quickly from very basic old computers used in big research facilities to a wide range of systems used in our daily life: mobile phones, tablets, laptops, WiFi and the Internet, etc. In a similar way, PICs will revolutionize several fields including next generation telecommunication networks like the Internet or the mobile network.

PICs can drastically increase the capacity and reduce the cost and power consumption of networks. This will allow the streaming of 4K

content to your computer and smart TV or the development of the next generation mobile network (known as 5G) which will allow the implementation of new services like the self-driving car, telesurgery or portable virtual reality.

Progress and challenges

Significant progress has been made since last year when the work package was created. Some key points:

- New collaboration with the EPSRC Future Metrology Hub including the University of Huddersfield and the University of Loughborough
- New industrial partners including Lumerical and Seagate
- Reinforced links with University College London with an additional project and joint PhD student
- Reinforced links with the University of Sheffield with an additional joint PhD student
- Several invited seminars, visits and workshops

Work package 9 has produced the following papers:

- E. Le Boulbar, D. Hayes, H. Liu, N. Abadía et al., 'Temperature Dependent Behavior of the Optical Gain and Electroabsorption Modulation Properties of an InAs/GaAs Quantum Dot Epistucture'. ICTON 2019
- N. Abadía, et al., "CMOS-Compatible Multi-Band TE-Pass Polarizer," Opt. Express (2019)
- N. Abadía, et al. 'Novel Polarization Beam Splitter with High Fabrication Tolerance'. CLEO 2019

Continuation studies in CS research

Rounds 1, 2 and 3

During year 2, we released our first call for applications to our feasibility study fund. This fund, totalling £1M (full economic cost) was reserved for new studies which push the boundaries of CS research. The aim of funding these feasibility studies is to broaden the reach of the Hub by encouraging new academic and industry partnerships, whilst supporting new cutting-edge research which is complementarity to and aligns with Hub objectives.

We originally envisaged supporting up to 10 projects of average length of 7.5 months; however we have used the flexibility available to us to set out a more extensive strategy for engaging with new partners and delivering key performance indicators via feasibility study funding.

Funding plan

Our first funding round, the studies funded during which have concluded, called for applications of up to £40k (80% full economic cost) over 6 months. This was followed with an opportunity for successful round 1 studies to apply for up to £96k (80% full economic cost), with this funding intended to lead to and facilitate a large scale EPSRC or Innovate UK grant application with strategic alignment to the Hub.

This was followed by a third funding round, coordinated with funding calls from other Future Manufacturing Hubs in order to encourage the possibility for collaborations involving multiple Hubs. This provided an opportunity to apply for up to 50k (80% full economic cost). This final call invited new applications from areas that overlap

between the Hubs, strengthening the links amongst them and promoting interaction, as well as delivering value for money.

Evaluation of applications for funding

The Hub Management Board (MB) hold responsibility for awarding funding for feasibility studies and have taken the advice of the Hub's Strategic Advisory Board in assigning funding to applicants.

Applications for the first round of funding were prioritised for funding according to the delivery of new academic and industrial collaborators, and were then scored on:

1. Scientific Quality and Clarity
2. Potential Impact/Opportunity
3. Hub Alignment

These criteria were used to enable new academic collaborators to request funding for new and innovative research projects which were aligned to the Hub strategy.

Funded applications

Six studies were awarded round 1 feasibility study funding, and they began their journey with the Hub on 1st August 2018 and were 6 months in duration.

In the funding call that was subsequently released, to enable the most promising of these studies to continue their work with the Hub, 4 continuation studies were awarded and their studies commenced between August and October 2019, with durations between 12 and 18 months. These build on the successful feasibility studies and deliver additional key performance indicators for the Hub.

Continuation studies in CS research

Introducing the 4 Hub-funded Continuation Studies

In total the Hub previously invested £229,992 in 6 high-risk, 6 month novel studies during the first funding round. The details of these studies are detailed in the Hub’s 2019 annual report www.compoundsemiconductorhub.org

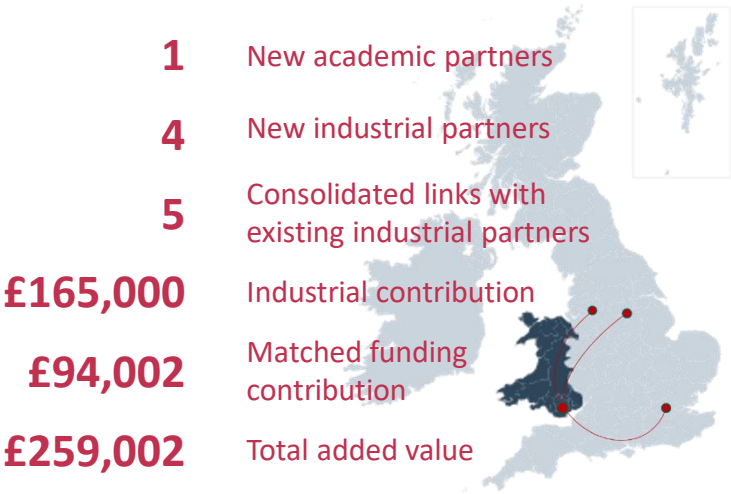
In 2019 the Hub invested £376,806 in the 4 continuation studies and the table and diagram below provide a summary of these projects; with detailed descriptions and outcomes for each project in the pages that follow this.

In 2020 the Hub invested a further £247,799 in 5 new studies as part of a joint feasibility call with other manufacturing Hubs. These projects are due to start in April 2020 and descriptions of these projects and their outputs will be included in the Hub’s 2021 report.

Details of the 4 Hub-funded continuation studies

PI	Institution	Title	Hub Mentor
Oleg Kolosov	Lancaster University	Three-dimensional mapping of active compound semiconductor structures	Tao Wang
Robert Taylor	University of Oxford	Angle edged etching of semiconductors (ACES)	Peter Smowton
Manus Hayne	Lancaster University	Semiconductor non-volatile RAM manufacture in Si substrates	Dave Wallis
Martin Kuball	University of Bristol	Nivel characterisation techniques for GaN RF electronic epitaxy	Paul Tasker

Summary of the continuation studies



Continuation study:

Three-dimensional structure and interfaces in compound semiconductors. Understanding links between electronic properties, defects, morphology and growth.

Lead applicant: Prof Oleg Kolosov, Lancaster University

Partners: Bruker UK Ltd, Lancaster Materials Analysis Ltd, Leica GMBH.

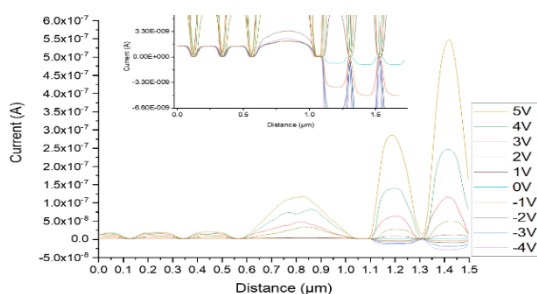
Hub Mentor: Tao Wang

Summary

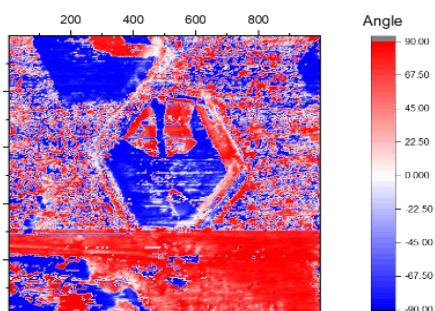
The project builds on the success of Lancaster University-led feasibility study that pioneered technology for three-dimensional (3D) nanoscale exploration of physical properties of compound semiconductor (CS) materials and devices by combining Lancaster invented wide area Ar-ion nanoscale Beam Exit Cross-sectional Polishing (BEXP) and Bruker multifunctional Scanning Probe Microscopy (SPM). The BEXP-SPM complements existing methods of bulk measurements (carrier transport, photoluminescence) and electron microscopy morphology mapping with the unique capability of mapping local nanoscale physical properties. We join efforts with industrial partners (Bruker, LEICA and LMA) and expand interaction with CS Hub collaborators (Sheffield, Cardiff, UCL, Manchester) to link nanoscale physical properties of buried internal layers of CS structures and devices to their performance, growth recipes and device reliability.

Outcomes/major findings

Together with Hub colleagues working on the design and manufacturing of Vertical Cavity Surface Emitting Lasers (VCSEL) we combined BEXP-SPM local electrical transport and nanoscale electrical potential measurements with FEA simulation to reveal 3D distribution of charge carriers, and current pathways in VCSEL devices mapping local doping and charge density



VCSEL (Cardiff). Point contact-to-electrode current vs x-section coordinate, (bottom) x-section spreading resistance microscopy SPM image, (inset) optical image of the sample

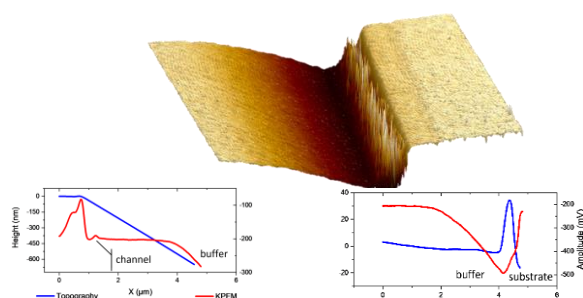


across the device, including a key active area with a few nanometres wide multiple quantum wells. This approach was also successfully applied to mapping of doping in the 10 μm thick p-i-n high energy particles detectors. The ongoing work focuses on the high angle BEXP sections of VCSEL devices to reveal oxide aperture shaping the current flow, and understanding the nanoscale origins of device lifecycle limitations.

With Hub colleagues working on the growth of III-N on silicon, we developed quantitative nano-mapping of the crystalline polar axes within iii-nitride nanowires (NWs) on Si using simultaneous vertical and lateral piezo-force microscopy (PFM), essential for developing high performance iii-nitride devices. By combining mapping of potential gradient across few nm thick Al-rich interface between Si substrate and NW and the FEA simulation, we recovered the charge density profile in this growth-defining zone. Using PFM we are also now piloting a 3D mapping of the UCL grown iii-v-on-Si structures targeting direct observation of APD defects via the orientation of piezoelectric moduli in the adjacent domains.

Relevance to manufacturing

The combination of application and fundamental science in this study provides powerful methodology for understanding the impact of nanoscale features of CS devices on their performance, allowing rational design of the device and selecting the optimal processing conditions. The examples include growth and annealing temperature optimisation, interfacial layer thickness and composition (iii-v on Si, iii-nitride NWs), selection of processing parameters (aperture oxidation in VCSELs) and revealing mechanisms of the device degradation (VCSELs, edge emitting iii-v lasers). The advancing BEXP-SPM has high potential for a broad field of CS manufacturing including HEMT devices, photodetectors and lasers.



iii-nitride NWs (Sheffield). (top) SEM image, (bottom left) BEXP section schematics, (right) NW polar axis orientation angle via piezoforce microscopy (PFM).

Continuation Study:

Angled-Cage Etching of Semiconductors (ACES)

Lead applicant: Prof Robert Taylor, Oxford University

Contributing academics: Dr Anthony Bennett, Dr JP Hadden, Dr Daryl Beggs (Cardiff), Prof Rachel Oliver, Dr Tong Tong Zhu (Cambridge)

Partners: Poro Technologies, Seren Photonics* (*in administration), Cardiff University

Hub Mentor: Peter Smowton

Summary

Modern semiconductor nanofabrication techniques can be used to create three-dimensional device geometries that support integrated photonic, electronic and mechanical functionalities. In silicon, the Bosch process can create devices with deep vertical sidewalls with an anisotropic etch or undercut surface layers using an isotropic etch. An open challenge is creating similar devices in wide-band-gap semiconductors that may operate in the visible spectral range. A promising technique is the use of angled dry etching to create suspended beams by placing the sample inside a Faraday cage in an Inductively Coupled Plasma (ICP) chamber. The Faraday cage deflects the ions causing them to impact on the sample at steep angles, removing material beneath a masked area. This study is targeting gallium nitride (GaN) heterostructures containing bright light sources for integrated photonics.

Outcomes

We have developed a single-step Faraday-cage assisted etch to create suspended nanostructures in gallium nitride (GaN). We have shown the Faraday cage can change the angle of etched sidewalls from +15° to -45°, which we have used to create suspended nanobeams and disc resonators.

novel angled etching technique to fabricate a nanocavity laser, using custom-grown material from our new project partner in Cambridge University's Centre for Gallium Nitride. Devices will be processed in Cardiff's Institute for Compound Semiconductors cleanroom and characterised in Oxford University. We will use photonic crystal cavity designs with a high quality-factor and small mode volume, tailored to our unique angled etching technique, to create a device with low lasing threshold. A new commercial partner, Poro Technologies, will contribute expertise in electro-chemical etching of GaN to improve side-wall roughness in our devices. We have calculated the waveguide dimensions that are required to achieve single mode guiding (b,c) and created initial photonic crystal devices based on waveguides with periodically modulated widths (d).

Relevance to manufacturing

The Faraday cage assisted etch allows us to control the etch angle, creating devices with new functionalities and novel designs. We have pursued a "single step" etch process to reduce costs. Data obtained from the Feasibility study has been used to support a successful application for an EPSRC manufacturing-fellowship.

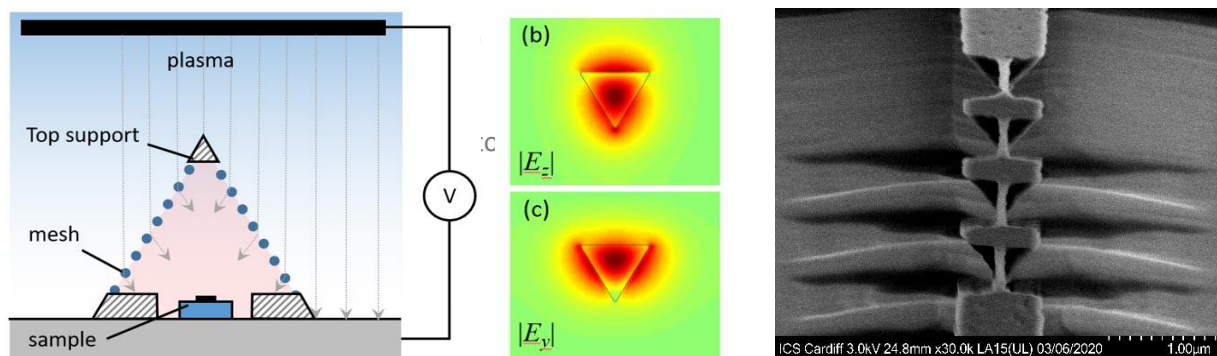


Figure: (a) cross-sectional cartoon of a Faraday Cage within the ICP etch chamber, which deflects ions to be incident on sample at a steep angles from either side. (b,c) electric field profiles of fundamental guided modes within triangular GaN waveguides. (d) SEM of a GaN triangular sections suspended by thin support wires, imaged at a steep angle.

Continuation study:

Feasibility of Compound Semiconductor Non-volatile RAM Manufacture on Si Substrates

Lead applicant: Prof Manus Hayne, Lancaster University

Partners: University of Warwick, IQE, Lancaster Material Analysis, EM Analysis, IMEC

Hub Mentor: Dave Wallis

Summary

The technology behind silicon-based processor and memory chips at the heart of all computers and electronic devices emerged in the 1970s. The memory chips – known as dynamic random access memory (DRAM) – are fast, but volatile, meaning that information is lost unless it is refreshed multiple times per second. Furthermore, when data is read from DRAM it is destroyed (destructive read), and needs to be reprogrammed, which is inconvenient.

In this project we are working towards the manufacturability of an innovative and completely new type of memory, one which fully exploits the opportunities for quantum engineering of materials and devices that are available in the compound semiconductor family. These memories are expected to be as fast as DRAM, but are non-volatile and with non-destructive read (NVRAM). Furthermore, despite this intrinsic robustness, the energy needed to write or erase the data is substantially lower than for DRAM. Computers and electronic gadgets of the future using such memories would be fast, boot-free (instantly on or off) and consume significantly less power.

Outcomes/major findings

The focus of the study is two-fold: (i) implementing the compound semiconductor memories on silicon (Si), and (ii) advancing from single-bit devices to small arrays. Compound semiconductor growth on Si is challenging because of the mismatch in crystalline lattices, thermal expansion coefficients and the change from elemental (Si) to compound semiconductors. In the feasibility study we combined different layers of materials for the first time, growing gallium antimonide (GaSb) on gallium arsenide (GaAs) on germanium (Ge) on silicon (Si). Whilst that was sufficient to demonstrate feasibility, we are now also investigating the growth of GaSb on

Si with an ultrathin layer of aluminium antimonide (AlSb) at the interface to compensate for the lattice mismatch. Concerning arrays, significant progress has been made with the fabrication of 4-bit devices (see image below), although they have not yet been successfully tested. We have also secured extra funding in the form of a high-profile EC ATTRACT project and an EPSRC Impact Acceleration Account award with industrial co-funding.

Relevance to manufacturing

The development and commercialisation of a new memory technology is a gargantuan task. This is demonstrated by phase change memory, which was first explored in the 1960's, but has only very recently seen commercial success in the form of Intel's Optane memory. Lancaster's compound semiconductor memory has been tested in single device (bit) format, with small (2x2) array fabrication in progress. To achieve cost-competitive manufacturing requires shrinking the devices to the nanoscale, exponentially increasing the number of bits on a chip, and implementation on industry-standard 300 mm Si wafers that are compatible with existing microelectronics chip production facilities.

In this project we are exploring two of those requirements, whilst the third, device scaling, will be investigated in parallel with separate funding. The ambitious medium-term aim is a 1 Mbit array on Si with integrated III-V CMOS addressing logic.



Two 2x2 (4-bit) ULTRARAM™ arrays with 20 nm feature size.

Continuation study:

New Characterisation Techniques for GaN RF Electronic Epitaxy

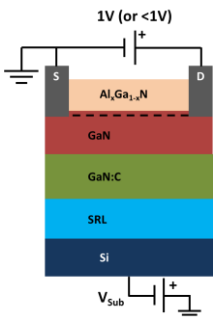
Lead applicant: Prof Martin Kuball, University of Bristol
Partners: Diamond Microwave Devices, IQE
Hub Mentor: Paul Tasker

Summary

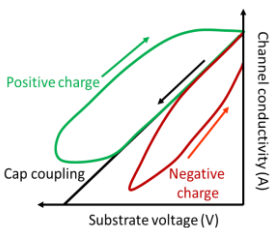
Compound Semiconductor gallium nitride (GaN) electronic devices used for monolithic microwave integrated circuit (MMIC) or discrete power applications require semi-insulating GaN epitaxial buffers which dramatically impact their performance in terms of important parameters such as short-channel effect, and current-collapse, as well as breakdown and leakage. In collaboration with industry, the Centre for Device Thermography and Reliability (CDTR) at Bristol University pioneered a new substrate ramp technique to characterise and optimise these GaN buffers. Working with IQE PLC and the Future CS Hub, the study concentrated on GaN-on-Si based epitaxy and scoped the feasibility of straightforwardly implementing this new approach in a manufacturing context. The study used “leaky dielectric” models of the epitaxial layers to understand trapping and leakage in the buffer. This is critically important for the establishment of an internationally competitive RF manufacturing process within the CSC.

Outcomes/major findings

A fast and simple route for feedback to epitaxial growers without complete device fabrication was demonstrated using simple test structures. An example comparison was undertaken of two different epitaxial designs, with quite distinct trapping behaviour observed both across the wafers and between wafers. The results were used to qualitatively predict the impact of the epitaxy on final device RF efficiency and power density. The approach and results were presented at the Reliability of Compound Semiconductors Workshop (ROCS 2019) in Minneapolis in April.



To test a GaN-on-Si epitaxial stack, a bi-directional voltage ramp is applied to the Si substrate and the channel conductivity is measured.

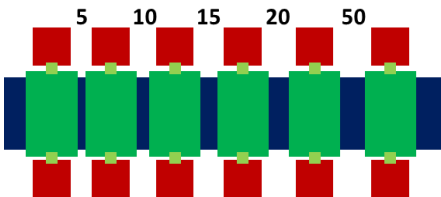


Epitaxy conduction mechanisms and charging can be sensed using the channel conductivity.

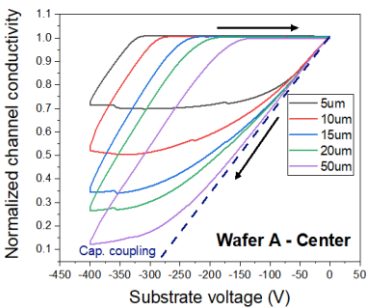
Since the start of the continuation study we defined jointly with IQE epilayer structure designs (confidential) of interest / suitable for this study. We also defined and designed specific test structures (confidential) to be fabricated and performed analysis on predicted outcomes and analysis methodologies; wafers were delivered early in 2021 by IQE following the earlier agreed specification and have been delivered to CSC Hub for fabrication. The wafers are at present being processed into the test structures we defined. Further measurements will then begin back in the CDTR.

Relevance to manufacturing

Traditionally radio frequency (RF) epitaxy can only be qualified by full device fabrication and test. The substrate ramp technique can provide feedback on material quality in a fraction of the time, dramatically shortening process development times, and vastly reducing the cost involved.



Simple fast-turnaround test structures fabricated at ICS.



Example data showing positive charging during the voltage ramp, and no remaining charge after the substrate voltage returns to zero. This is characteristic of good epitaxy.

Key performance indicators

Annual and long-term targets to measure success

The CS Hub has a number of targets formed of measurable research outputs that are carefully designed to measure the success of the Hub in the context of the CS research environment. Many of these targets are only possible to achieve in the long-term, while others can demonstrate more immediate success for the Hub. The Key performance indicators (KPIs) for the Hub are detailed below. The following page contains some of the Hub’s key achievements for these KPIs.

KPI	Success criteria
New industrial partners, based on exciting manufacturing challenges	5 per annum
New universities joining	5
Close collaborative links with other EPSRC Manufacturing Hubs and the EPSRC Centre for III-V Technology	Joint activities / events
Close collaborative links between the hub and major complementary overseas centres of excellence such as MIT, IMEC or NTU Singapore	2 over duration of Hub
Compound Semiconductor training centre activities to include: a) university and industry funded doctoral level training, b) MSc courses c) on-job and/or apprenticeship training to support industry d) summer schools for postdocs and PhD students	Delivery of a number of training activities per annum
Research and industrial awards per year for associated activity	Average of £5.5M (100% FEC) per annum
Conference presentations per year	Average of 10 per annum
Publications per year	Average of 20 per annum
Commercial impact activity to include: a) Number of IP disclosures/patents filed. b) Number of IP licences granted. c) Amount of VC funding generated, based on Hub technologies. d) New product roll-outs from partners, based upon Hub technologies. e) Sales value enabled by Hub technologies.	This is a late/lagging indicator and can be used later in the project to monitor success.
Outreach activity to include training	Delivery of a number of outreach activities per annum
Career development of Hub staff	Demonstration of staff development via securing fellowships, career training, etc.

The Year in Numbers

Based on our Key Performance Indicators, and some other important measures of success, we have generated some impressive numbers at the Future CS Hub.

82

Publications

Conference presentations & abstracts

Including 31 keynote and invited speakers.

161

56

Collaborations & partnerships

Further funding

Including 5 new awards.

33

42

Outreach & engagement

Including industrial events, international seminars and conferences.

Training activity

18

8

Impact

Including 1 spin off company and 7 patent applications.

Career development

9

22

Links to other hubs and centres overseas

Outreach

The Hub has further expanded its outreach activity

As in previous years, the last year has seen a wide range of Hub outreach activity. Our engagement has extended to the academic community; Industry partners; Hub cluster partners (ICS, Catapult, CSC) and Manufacturing Hubs and research groups. In addition to this, we have widened our web presence and learning and development activity.

Joint Feasibility Study with other Hubs

As described above, the Hub has invested in a number of feasibility studies and most recently this has been done as part of a joint feasibility call with other manufacturing Hubs. We worked together closely to agree the scope of the call and the priority areas identified by each of the four partner Hubs; in addition to coordinating the joint processing of applications and the delivery of the projects involving multiple partners.

New Outreach Officer

The Hub has recently recruited a new Outreach Officer, Grace Mullally, who over the next year and beyond will be working on reaching non-CS specialist audiences, with a focus on outreach with primary schools and the accessibility of careers in CS to all groups.

Hub engagement with Industry

Over the past year we have worked with industry partners in a number of ways and in accordance with TRL evolution of the Hub's work. This includes engaging with key partners such as the Welsh Assembly Government; industry partners providing PhD sponsorship for Hub students; and strategic partnerships to support specific elements of Hub research with companies such as Renishaw and TWI.

The Hub ran an industry day in September 2019 which also incorporated the new Centre for Doctoral Training (CDT) and was attended by key partners, including the National Physical Laboratory, Compound

Semiconductor Technologies and Airbus. The Hub Director provided a presentation on the CS ecosystem and the Hub's work with academia and industry. There were accompanying presentations on the Hub's research and a networking session for the Hub and industry partners. In January 2020 Sheffield also ran the Centre for GaN Materials and Devices Industry Open Day.

Website and Twitter

Our Hub website (<http://compoundsemiconductorhub.org>) continues to evolve with our flexible program of work and our Twitter feed (@FutureCSHub) has also grown this year to over 300 followers. It is being used regularly by our colleagues, for example the Institute for Compound Semiconductors (ICS), Ser Cymru Research Group and the GaN Centre (University of Sheffield) to advertise opportunities such as conferences, PhD studentships and advertised posts.

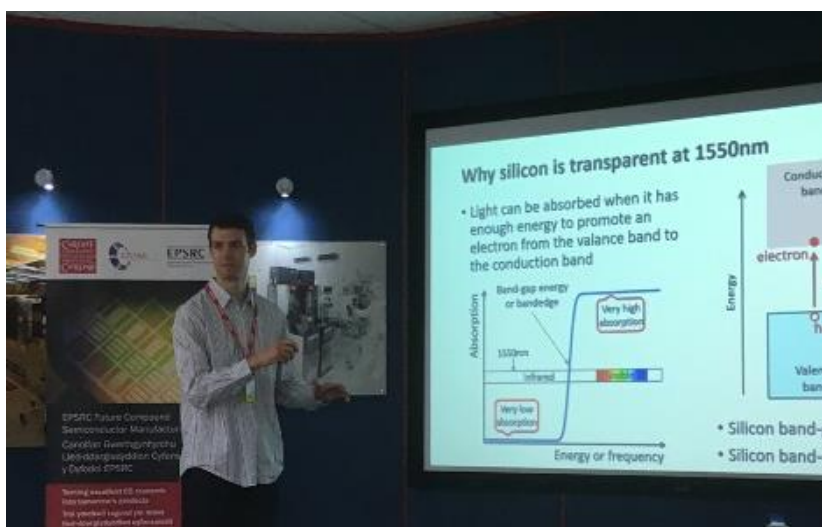
Conferences

In April 2019, the Semiconductor and Integrated Optoelectronics Conference (SIOE) took place in Cardiff. The Hub also had a stand at the UK Semiconductor Conference in Sheffield in July 2019 and was represented at the Photonics West Conference in San Francisco in January 2020.

Training

During the last year the Hub has developed and delivered unconscious bias training for staff from across the Hub and project management training for Hub staff and students from the CDT. A learning and development survey was also developed to ascertain current and future leaning needs amongst staff and will inform the Hub's learning and development plans and expanded training programme for the year ahead.

Outreach

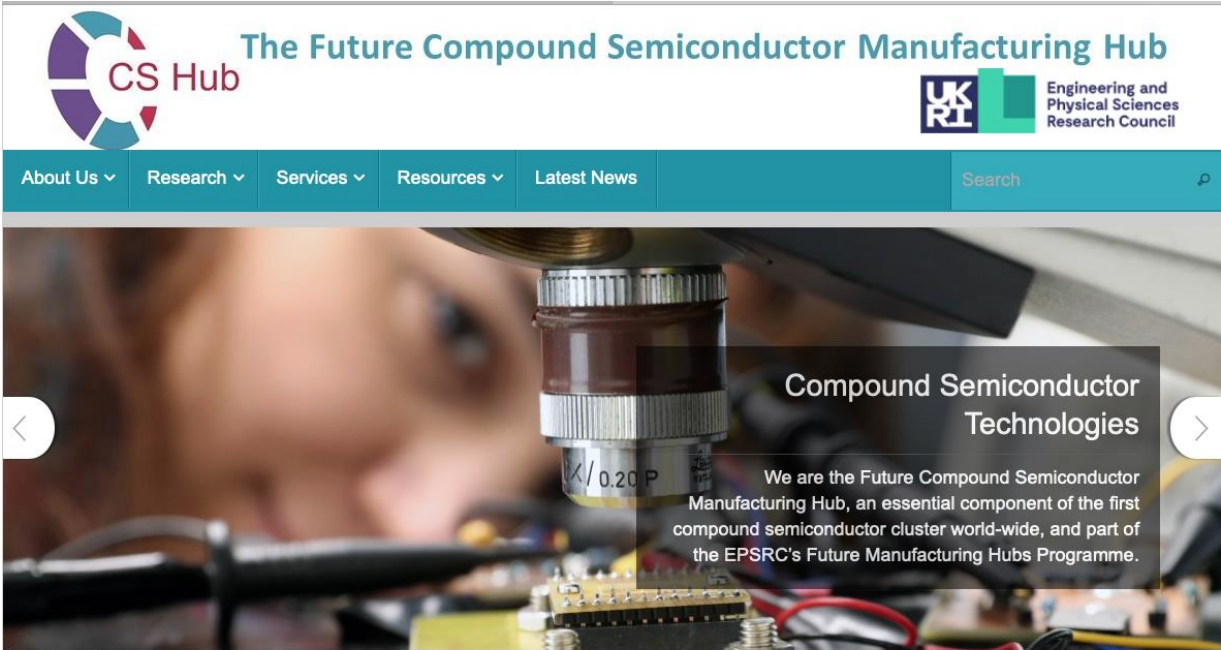


Images (top to bottom): the SIOE conference in Cardiff; Dr Daryl Beggs providing training at Newport Wafer Fab at the Compound Semiconductor photonic and electronics workshop sponsored by the CS Hub; and the GaN Materials and Devices Industry open day in Sheffield.

Outreach



CS hub Twitter page @FutureCSHub which has grown to over 300 hundred followers this year.



The landing page of the CS Hub website www.compoundsemiconductorhub.org

Research output: Publications

Peer reviewed publications are a key indicator of our research success

Publications are a vital measure of success for the Hub and we aim to develop as much high quality, unique and useful research as possible in the CS field. In last year's annual report we were able to include 14 new publications for the CS Hub.

This year we are able to report the publication of several new key research findings from all 4 original CS Hub academic partners (Cardiff University, the University of Manchester, the University of Sheffield and University College London).

3D ITO-nanowire networks as transparent electrode for all-terrain substrate. Wang, Z; Li, Y; Ding, W *et al.* Scientific Reports. 2019:9:4983. DOI: 0.1038/s41598-019-41579-2

Achieving wavelength emission beyond the C-band from Type-II InAs-GaAsSb quantum dots grown monolithically on silicon substrate. Salhi A, Alshaibani S, Alaskar Y, *et al.* Journal of Alloys and Compounds. 2019: 771, pp382-386. DOI: 10.1016/j.jallcom.2018.08.276

Altering the Optical Properties of GaAsSb-Capped InAs Quantum Dots by Means of InAlAs Interlayers. Salhi A, Alshaibani S, Alaskar Y, *et al.* Nanoscale Research Letters. 2019: 14:41. DOI: 10.1186/s11671-019-2877-2

Cathodoluminescence studies of chevron features in semi-polar (112-2) InGaN/GaN multiple quantum well structures. Brasser C, Bruckbauer J, Gong Y. P. *et al.* Journal of Applied Physics. 2018:123:174502. DOI: 10.1063/1.5021883

Confocal photoluminescence investigation to identify basal stacking fault's role in the optical properties of semi-polar InGaN/GaN lighting emitting diodes. Zhang Y, Smith R. M, Jiu L, *et al.* Scientific Reports. 2019: 9, pp 9735. DOI: 10.1038/s41598-019-46292-8

Demonstration of Si based InAs/GaSb type-II superlattice p-i-n photodetector. Deng Z, Guo D, Burguete C.G, *et al.* Infrared Physics & Technology. 2019:101, pp 133-137. DOI: 10.1016/j.infrared.2019.06.011

Determining GaN nanowire polarity and its influence on light emission in the scanning electron microscope. Naresh-Kumar G, Bruckbauer J, Winkelmann A, *et al.* Nano Letters. 2019:19:3863. DOI: 10.1021/acs.nanolett.9b01054

Flexibility of Ga-containing Type-II superlattice for long-wavelength infrared detection. Delmas M, Kwan D, Liang B. L. *et al.* Journal of Physics D: Applied Physics, 2019:52:47. DOI: 10.1088/1361-6463/ab3b6a

Growth mechanisms for InAs/GaAs QDs with and without Bi surfactants. Chen X.Y, Gu Y, Ma M.J, *et al.* Materials Research Express. 2018: 6:1, pp015046. DOI: 10.1088/1555-6611/aae194

Heavily tin-doped indium oxide nano-pyramids as high-performance gas sensor. Li Q, Zhang Y, Wang Z, *et al.* AIP Advances . 2018:8:115316. DOI: 10.1063/1.5048622

Research output: Publications

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Integration of III-V lasers on Si for Si photonics. Progress in Quantum Electronics. Tang M, Park J-S ,Wang Z , *et al.* Processes in Quantum Electronics. Volume 66, August 2019, Pages 1-18. DOI 10.1016/j.pquantelec.2019.05.002

Investigation of growth parameters influence on self-catalyzed ITO nanowires by high RF-power sputtering. Jiu L, Gong Y and Wang . Nanotechnology. 2018:29:165708. DOI: 10.1088/1361-6528/aaafa7

ITO nanowires grown on Ni foam as voltage self-stabilizing supercapacitor electrode. Li Q, Wang Z, Zhang Y, *et al.* Journal of Materials Research. 2019:34, pp 3195-3203. DOI: 10.1002/anie.201410050

Low-cost InP–InGaAs PIN–HBT-based OEIC for up to 20 Gb/s optical communication systems. Muttlak S.G, Kostakis I, Abdulwahid O.S *et al.* IET Optoelectronics. 2019:13:3, p144 – 150. DOI: 10.1049/iet-opt.2018.5032

Monolithic multiple colour emission from InGaN grown on patterned non-polar GaN. Gong Y, Jiu L, Bruckbauer J, *et al.* Scientific Reports. 2019:9:986, DOI 10.1038/s41598-018-37575-7

Monolithically integrated white light LEDs on (11-22) semi-polar GaN templates. Poyiatzis N. Athanasiou M , Bai J, *et al.* Scientific Reports. 2019:9:986. DOI: 10.1038/s41598-018-37008-5

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Non-polar (11-20) GaN grown on sapphire with double overgrowth on micro-rod/stripe templates. Bai J, Jiu L, Gong Y and Wang T. Semiconductor Science and Technology. 2018: 33; 12. DOI:10.1088/1361-6641/AAED93

Optical and polarisation properties of nonpolar InGaN-based light-emitting diodes grown on micro-rod templates. Bai J, Jiu L, Fletcher P, *et al.* Scientific Reports. 2019:9, pp 9770. DOI: 10.1038/s41598-019-46343-0

Origin of defect tolerance in InAs/GaAs quantum dot lasers grown on silicon. Liu Z, Hantschmann C, Tang M, *et al.* Journal of Lightwave Technology. 2019, P 1-1, DOI: 10.1109/JLT.2019.2925598

Overgrowth and strain investigation of (11-20) non-polar GaN on patterned templates on sapphire. Jiu L, Gong Y and Wang T. Scientific Reports 2018:8:9898. DOI 10.1038/s41598-018-28328-7

Research output: Publications

Physical modelling of InGaAs-InAlAs APD and PIN photodetectors for > 25 Gb/s data rate applications. Abdulwahid O.S, Kostakis I, Muttalak S. G, *et al.* IET Optoelectronics. 2019:13:1, pp40-45. DOI: 10.1049/iet-opt.2018.5030

Recent progress in epitaxial growth of III-V quantum-dot lasers on silicon substrate. Pan S, Cao V, Liao M, *et al.* Journal of Semiconductors. 2019:40:101302. DOI: 10.1088/1674-4926/40/10/101302

Scanning electron microscope as a flexible tool for investigating the properties of UV-emitting nitride semiconductor thin films. Trager-Cowan C, Zhang Y, Jiu J, *et al.* Photonics Research. 2019:7:B73. DOI:10.1364/PRJ.7.000B73

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Semi-polar InGaN-based green light-emitting diodes grown on silicon. Shen S, Zhao X, Yu X, *et al.* Phys. Stat. Sol, (A). 2019: 1900654. DOI:10.1002/pssa.201900654

Surface-breaking flaw detection in mild steel welds using quan-tum well hall effect sensor devices. Watson J.M, Liang C.W, Sexton J, *et al.* AIP Conference Proceedings. 2019: 2102: 080010. DOI: 10.1063/1.5099818

The effect of post-growth rapid thermal annealing on InAs/InGaAsdot-in-a-well structure monolithically grown on Si. Li W, Chen S, Wu J, *et al.* Journal of Applied Physics. 2019:125: 135301 DOI: 10.1063/1.5085175

Ultra-Energy-Efficient Photoelectrode Using Microstriped GaN on Si. Syed Z.A, Hou Y, Yu X, *et al.* ACS Photonics. 2019:6; 1302-1306. DOI 10.1021/acsphotonics.9b00478

Ultra-low threshold InAs/GaAs quantum dot microdisk lasers on planar on-axis Si (001) substrates. Zhou T. Tang M, Xiang G *et al.* Optica. 2019:6:430. DIO:10.1364/OPTICA.6.000430

Research output: Conference presentations

Conference presentations and abstracts delivered by the Hub

Our researchers have been extremely proactive in delivering high quality, peer reviewed research. A great deal of this has been reported in conference publications, via invited talks, abstract presentations and keynote speeches. We are confident that in the following years, these conference outputs will translate into full publications wherever possible.

12.5 GHZ InP Quantum Dot Monolithically Mode-Locked Lasers Emitting at 740nm. Li Z and Allford C. CLEO 2019. Munich, Germany, 23rd -27th June 2019.

24GHz Zero-Bias Asymmetrical Spacer Layer Tunnel Diode Detectors. Abdulwahid O, Muttalak S, Sexton J, *et al.* UCMMT 2019, Queen Mary University, UK, 20th – 22nd August, 2019.

An Integrated Optoelectronic Microfluidic Platform for Particle Manipulation and Control. Giliyana D, Gillgrass S-J, Almagwashi B, *et al.* UK Semiconductors, Sheffield Hallam University, UK, 10th – 11th July 2019.

Characterization of gain and loss of In(Ga)As/GaAs quantum dot active region for high temperature operation. Le Boulbar E, Jarvis L, Hayes D, *et al.* UK Semiconductors, Sheffield Hallam University, UK, 10th – 11th July 2019.

Dependant Characteristics of p-doped Laser Devices. Jarvis L, Shutts S, Tang M, *et al.* UK Semiconductors, Sheffield Hallam University, UK, 10th – 11th July 2019.

Designing optimized retro-reflecting electro-absorption modulators for free space optical datalinks. Maglio B and Abadia Cavo N. Semiconductor and integrated optoelectronics conference (SIOE), Cardiff, 16th -18th April, 2019.

Development of Semi-Polar (11-22) GaN for Green Emitters on Si Substrates. Yu X, Shen S.H, Zhao X. M, *et al.* International Conference on Nitride Semiconductors. Washington, USA, 7th – 12th July 2019.

Experimentally Validated Physical Modelling of Asymmetric Spacer Layer Tunnel Diodes for THz Applications. Hadfield A, Salhi A, Sexton J and Missous M. The 12th UK/Europe-China Workshop on Millimetre-Waves and Terahertz Technologies (UCMMT) Queen Mary University, UK, 20th – 22nd August, 2019.

Explore semi-polar/non-polar GaN for future photonics and Electronics (Keynote talk). Wang T. International Conference on Optoelectronic and Microelectronic Technology and Application 2019, Nanjing, China, 7th -9th November 2019.

Growth and characterization of long-wavelength Type-II InAs/GaSb superlattice infrared detectors, Kwan D.C.M, Delams M, Liang B and Huffaker D. Semiconductor and integrated optoelectronics conference (SIOE), Cardiff, 16 – 18th April 2019.

High-performance III-V lasers monolithically grown on Si substrates. Deng H, Liao M, Pan S, *et al.* Gettering and Defect Engineering in Semiconductor Technology 2019, Berlin, Germany 22-27th September 2019

Research output: Conference presentations

High-performance III-V lasers monolithically grown on Si substrates (Invited). Yang J, Liu Z, Tang M, *et al.* PIERS 2019, Xiamen, China, 17th – 20th December, 2019.

III-V Quantum Dot Lasers Monolithically Grown on Silicon (Invited talk). Liu H, OFC, San Diego, California, USA, 3rd – 7th March 2019.

InGaAs/AlAs Metamorphic Asymmetric Spacer Tunnel (mASPAT) Diodes on GaAs Substrate for Microwave/millimetre-wave Applications. Salhi A, Sexton J, Muttalak S.G, *et al.* The 12th UK/Europe-China Workshop on Millimetre-Waves and Terahertz Technologies (UCMMT), Queen Mary University, UK, 20th – 22nd August, 2019.

InGaAs/AlAs Resonant Tunneling Diodes with Very High Negative Differential Conductance for Efficient and Cost Effective mm wave/THz Sources. Muttalak S.G, Abdulwahid O.S, Sexton J and Missous M. UCMMT 2019, Queen Mary University, UK, 20th – 22nd August, 2019.

InP Quantum Dot Monolithic Mode-Locked Lasers for Ultrashort Pulse Generation at 735 nm. Allford C, Li Z, Sutts S, *et al.* ESLW 2019, Cork, Ireland, 27th - 28th September.

InP Quantum Dot Monolithically Mode-Locked Lasers Emitting at 740 nm. Li Z and Allford C. Semiconductor and integrated optoelectronics conference (SIOE), Cardiff, 16th -18th April, 2019.

Silicon-based III-V Quantum-dot Laser for Silicon Photonics. Wu J, Chen S, Tang M, *et al.* Asia Communications and Photonics Conference (ACP) 2019, Chengdu, China. 2th -5th November 2019.

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Luminescence and conductivity studies of chevrons in semi-polar (11-22) InGaN/GaN multiple quantum well structures. Brasser C, Bruckbauer J, Li Z, *et al.* International Conference on Nitride Semiconductors. Washington, USA, 7th – 12th July 2019.

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Material Characterization and Thermal Performance of Au Alloys in a Thin-Film Plasmonic Waveguide. Bello F, Orhan O, Abadia N, *et al.* Conference on Lasers and Electro-Optics (CLEO 2019). San Jose, United States. 5th – 10th May, 2019. DOI:10.1364/CLEO_AT.2019.JTu2A.110

Microstructural imaging of ferromagnetic material using integrated quantum well Hall-effect sensor arrays. Liang C-W, Sexton J, Sadeghi and Missous M. BINDT 2019, Teleford, uk. 3rd -5th September 2019.

Monolithic Growth InAs Quantum Dots Lasers on (001) Silicon Emitting at 1.5 μm . Li Z, Shutts S, Allford C, *et al.* UK Semiconductors, Sheffield Hallam University, UK, 10th – 11th July 2019.

Monolithic Growth of 1.5 μm InAs Quantum Dots Lasers on (001) Si and Material Studies. Li Z. Semiconductor and integrated optoelectronics conference (SIOE), Cardiff, 16th -18th April, 2019.

Research output: Conference presentations

Monolithic growth of InAs quantum dot lasers on (001) Silicon emitting at 1.55 μ m. Li Z, Shutts S, Allford C, *et al.* IPC 2019, San Antonio, Texas, USA, 29th September - 3rd October 2019.

Monolithic InP Quantum Dot Mode-Locked Lasers Emitting at 730 nm Waveband. Li Z, Allford C, Shutts S, *et al.* IPC conference 2019, San Antonio, Texas, USA, 29th September - 3rd October 2019.

Monolithic On-Chip Integration of HEMTs/Green LEDs. Cai Y, Gong Y, Bai J, *et al.* International Conference on Nitride Semiconductors. Washington, USA, 7th – 12th July 2019.

Optical Gain and Absorption of 1.55 μ m Emitting InAs Quantum Dot Lasers Directly Grown on (001) Silicon. Allford C, Li Z, Shutts S, *et al.* ESLW 2019, Cork, Ireland, 27th - 28th September

Plasmonic Integrated Multimode Filter. Abadia N, Samani A, Le Boulbar E, *et al.* 21st International Conference on Transparent Optical Networks (ICTON 2019). Angers, France. 9th – 13th July, 2019. DOI:10.1109/ICTON.2019.8840183

Roadmap of 1300-nm InAs/GaAs quantum dot laser grown on silicon for silicon photonics. Liu Z, Mengya L, Hantschmann C, *et al.* The International Photonics and Optoelectronics Meeting (POEM), Whuan, China. 11th -14th November 2019

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Si-based III-V Quantum Dot Lasers: the Solution of Laser for Si Photonics. Lui H. 13th Chinese National Silicon Photonics Conference, Hangzhou, China. June 2019.

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Temperature Dependent Behavior of the Optical Gain and Electroabsorption Modulation Properties of an InAs/GaAs Quantum Dot Epistucture. Le Boulbar E, Jarvis J, Hayes D, *et al.* 21st International Conference on Transparent Optical Networks (ICTON 2019). Angers, France, 9th -13th July, 2019. DOI:10.1109/ICTON.2019.8840542

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Research Highlight: CS Manufacturing (WP6)

Direct epitaxial growth to manufacture ultra-small and ultra-bright visible μ LEDs

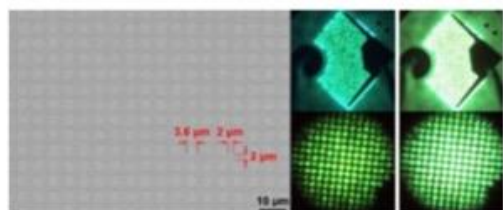
There is a significantly increasing demand for developing III-nitride compound micro light emitting diodes (μ LEDs) for high-speed visible light communications (VLC), micro-displays for smartphones and smart-watches and Augmented Reality and Visual Reality (AR & VR) applications. III-nitride μ LEDs exhibit a number of unique features compared with organic LEDs (OLEDs) and liquid crystal displays (LCDs), such as high resolution, high efficiency, fast carrier recombination lifetime, high contrast ratio, etc. Traditionally, III-nitride μ LEDs are exclusively fabricated by means of combining a standard photolithography technique and subsequent dry-etching processes, leading to severe damages unavoidably introduced by dry-etching processes and thus degradation in optical performance. This issue becomes increasingly severe with decreasing the dimension of μ LEDs. Therefore, so far there has been a near complete absence of reports on μ LEDs with a dimension of $<5\text{ }\mu\text{m}$, while such μ LEDs are the key components for high resolution micro-displays and VLC.

In order to overcome the great challenge, we have developed a *direct epitaxial approach to achieving ultra-small and ultra-bright visible μ LEDs by using a standard commercial MOVPE system, which can be easily transferred to industry for mass-production manufacturing with reduced costs and high yields.* Our approach is to employ selective overgrowth which takes places only within pre-patterned SiO_2 microhole arrays, where the dry-etching processes for the formation of μ LED mesas which are the unavoidable procedure in the conventional fabrication approaches have been completely eliminated. Consequently, μ LEDs with an ultra-high brightness of above 10^7 cd/m^2 and a record EQE of

6% in the green spectral region have been achieved. The results have been published in *ACS Photonics*, 7(2), 411-415 (2020), and have been highlighted quickly by a number of semiconductor magazines after publication. The results of this paper have directly led to the establishment of Sheffield's spin-out, EpiPix Ltd, dedicating to the manufacturing of an epitaxial integration of μ -LEDs and HEMTs. EpiPix Ltd was officially founded on 20th January 2020. Please also refer to very recent press below for the major technological breakthrough and EpiPix Ltd.

Highlights in Recent press

- 23rd January 2020, <https://www.eenewseurope.com/news/green-ingan-microleds-beat-all-efficiency-benchmarks>
- 6th February 2020, Materials World ["Developing micro-LED technology"](#)
- 12th March 2020, Compound Semiconductor, ["EpiPix: A New Way With Micro-LEDs"](#)
- 4th February 2020, The University of Sheffield ["New University of Sheffield spin-out company developing game-changing micro-LED technology"](#)
- 3rd February 2020, LED Inside ["University of Sheffield Spin-out EpiPix Developing Micro LED Technology for Next-gen Applications"](#)
- 3rd February 2020, Semiconductor Today ["University of Sheffield spins off EpiPix to develop and commercialize micro-LED technology"](#)
- 31st January 2020, Electronicsweekly.com ["University of Sheffield spin-out EpiPix developing micro-LEDs"](#)
- 31st January 2020, Compound Semiconductor, ["University Of Sheffield Spins-out Micro-LED Company"](#)



"SEM image of our μ LED array wafer showing a diameter of $3.6\text{ }\mu\text{m}$ and an inter-pitch of $2\text{ }\mu\text{m}$.

Emission microscopy images of our μ LED arrays at an injection current density of 3 and 9 A/cm^2 , respectively (upper: under a low magnification ; and bottom: under a high magnification;"

From ACS Photonics, 7(2), 411-415 (2020).

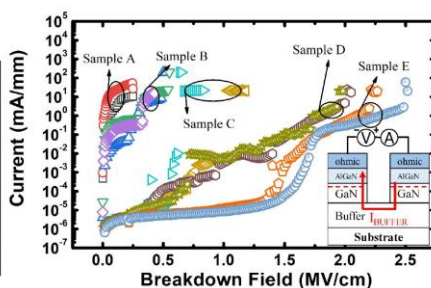
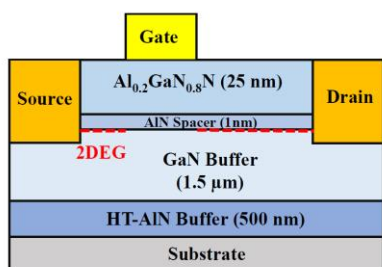
Research Highlight: Epitaxial Integration (WP6)

Monolithic on-chip epitaxial integration of III-nitride μ LEDs and HEMTs for Li-Fi

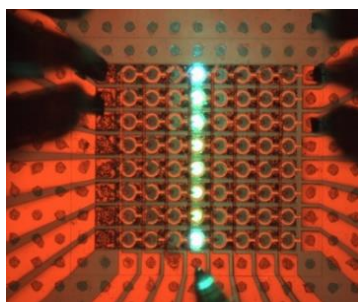
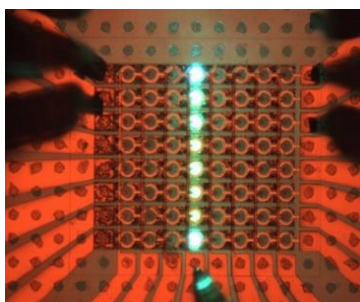
Integration of compound semiconductor electronics and photonics is the possible ultimate approach to manufacturing semiconductor devices with multiple and diverse functions. A number of methods have been proposed, such as wafer-transfer technologies which involve complicated substrate lift-off and transfer-print processes, significantly increasing manufacturing costs and reducing manufacturing yields. This fundamental issue could be resolved by developing monolithic on-chip integration of electronics and photonics on a single wafer by direct epitaxy, namely, monolithic on-chip epitaxial integration. In this case, this requires a more advanced epitaxial growth technique than standard epitaxial growth methods, in particular, large lattice-mismatched hetero-epitaxial growth techniques which need to be developed. Furthermore, the advanced epitaxial growth of both electronics and photonics will also have to be established. For example, the electronic component of such an integration system requires much higher performance than those for standalone case applications. This is particularly important for III-nitride compound semiconductor electronics and photonics grown on either widely used silicon or sapphire substrates.

developed a novel two-dimensional epitaxial growth mode benefiting from our well-established high-temperature AlN buffer technology using metalorganic vapour phase epitaxy growth (MOVPE) which is different from the classic two-step approach to the epitaxial growth of III-nitride compound semiconductors. As a result, we have achieved high electron mobility transistors (HEMTs) with exceptional performance, demonstrating a record high breakdown field of 2.5 MV/cm approaching the theoretical limit of GaN (3 MV/cm) and an extremely low off-state buffer leakage of 1 nA/mm at a bias of up to 1000 V. Furthermore, our HEMTs also exhibit an excellent figure-of-merit ($V_{br}^2/R_{on,sp}$) of $5.13 \times 10^8 \text{ V}^2/\Omega \cdot \text{cm}^2$. The results have been published in *ACS Appl. Mater. Interfaces* 12,12949-12954 (2020).

We have applied the novel epitaxial growth technique in manufacturing III-nitride compound monolithic epitaxial integration, demonstrating the 1st monolithic on-chip epitaxial integration of μ -LEDs and HEMTs with a modulation bandwidth of >1 GHz for Li-Fi.



Our HEMTs exhibit a record high breakdown field of 2.5 MV/cm, an extremely low off-state buffer leakage of 1 nA/mm at a bias of up to 1000 V and an excellent figure-of-merit ($V_{br}^2/R_{on,sp}$) of $5.13 \times 10^8 \text{ V}^2/\Omega \cdot \text{cm}^2$. From *ACS Appl. Mater. Interfaces* 12, 12949-12954 (2020).



“Optical microscopy photographs show our monolithic on-chip epitaxial integration of μ -LEDs and HEMTs during operation, where the HEMTs are used to control μ -LEDs, leading to a modulation bandwidth of >1 GHz.” From a manuscript under peer review.



Centre For
GaN
Materials and Devices



The
University
Of
Sheffield.



New award highlight: GaNforCS

Developing GaN on SiC RF devices for 'next generation' technologies

Gallium Nitride for Communications and Security (GaNforCS) is an industry-driven project funded through Welsh Government's SMARTExpertise programme, with the aim of establishing a UK supply chain for RF-GaN active and passive devices and accelerating the development of the important integrated chipset technologies needed to support the high performance requirements of emerging applications in communication (5G and beyond), radar and satellite systems. Hub Research activities relating to the development of wafer-level testing and characterisation will be important to support ongoing activities for this award.

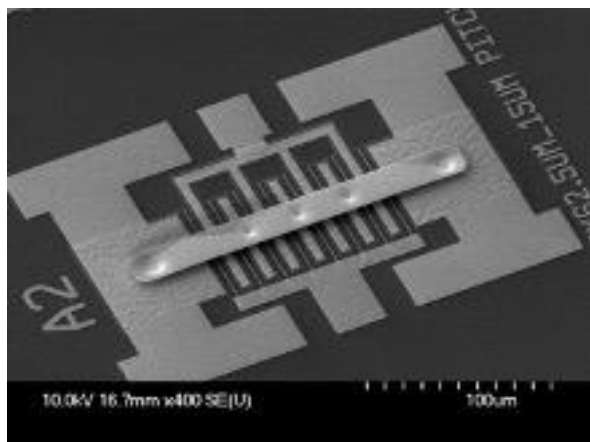
Compared to silicon, RF-GaN offers higher operating frequencies, simplified circuit design, lower power and improved efficiency, higher temperature tolerance, as well as supporting both active and passive devices. These remarkable properties mean that GaN can be used to create exceptionally fast devices or chips that form critical components in telecommunication (5G and beyond), security and defence, radar, automotive, aerospace and satellite systems.

The proposed technology development builds upon the outcomes of a successful Innovate UK funded research project, led by the Centre for High Frequency Engineering (CHFE) at the School of Engineering, Cardiff University, and through which a stable internationally competitive GaN-on-SiC HEMT transistor device technology has been developed.

The GaNforCS consortium, led jointly by the CHFE and the Compound Semiconductor Applications Catapult (CSAC), is supporting and working alongside industrial partners within the Compound Semiconductor (CS) cluster, CSCConnected, to develop these devices. Involving most of the core CSCConnected partners, the project focusses on epitaxy, compound semiconductor fabrication, advanced characterisation, as well as production and test – with the potential to open doors to future collaborations, governance and IP sharing agreements.

The SMARTExpertise programme is part-funded by the European Regional Development Fund through the Welsh Government, which offers financial support to innovative collaboration projects between industry and Welsh research organisations. The programme addresses strategic industrial technical challenges with a clear focus on commercialisation and exploitation of new products, processes or services and growth in capacity and capability in key areas of Smart Specialisation.

GaNforCS partners include Cardiff University, The Compound Semiconductor Applications Catapult (CSAC), Newport Wafer Fab (NWF), SPTS, IQE, The Compound Semiconductor Centre (CSC), Leonardo, MBDA, Arralis, TT-Electronics, IconicRF, Filtronic and Focus Microwave group.



A CHFE millimetre-wave transistor based on a 250nm T-gate GaN On SiC HEMT process with a gain of 13 dB at 26 GHz.

New award highlight: Semiconductor industry - an ASSET to Wales

The ASSET project (Application Specific Semiconductor Etching Technology)

The ASSET project (Application Specific Semiconductor Etching Technology) is funded under Welsh Government's Smart Expertise programme and is an industrially driven, collaborative project with partners across South Wales including SPTS Technologies, IQE, the Compound Semiconductor Centre (CSC), Biovici, BioMEMS, plus Swansea and Cardiff Universities, and Integrated Compound Semiconductors Ltd (Manchester). Hub Research activities will also be important to support activities for this award.

The ASSET industrial partners provide globally leading technologies which go into almost all the world's leading smartphones. By developing a host of new semiconductor process technologies, ASSET will develop these technologies for Compound Semiconductors and next generation semiconductor materials, to service new

emerging applications in automotive sensing, 5G, Photonics and Healthcare.

Kevin Crofton, President of SPTS Technologies added "The ASSET project gives the consortium the ability to work with the extensive fabrication supply chain in the region to further expand our capabilities and capitalise on new and exciting market opportunities".

CSC's Wyn Meredith continued "The South Wales semiconductor industry employs over 1400 highly skilled people in the region and is set to expand rapidly over the next 5 years with the development of 5G, AI and other mega-trend markets. ASSET will support these developments by developing a range of advanced semiconductor processes and expertise to overcome technical and industry challenges."



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