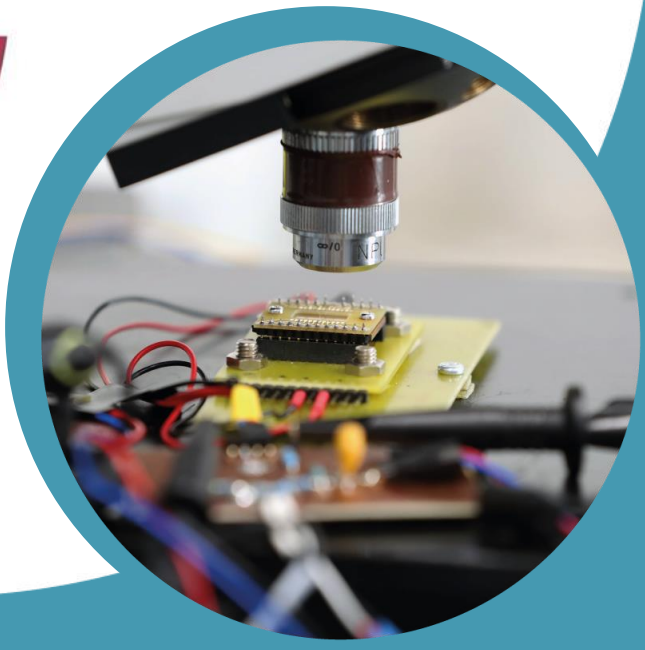
CS Hub



Future Compound Semiconductor Manufacturing Hub

Establishing the UK as the primary global CS research and manufacturing hub

Annual Report 2019

The Future Compound Semiconductor Manufacturing Hub EPSRC grant number EP/P006973/1

EPSRC
Engineering and Physical Sciences Research Council

EPSRC Future Manufacturing Research Hubs

compoundsemiconductorhub.org
@FutureCSHub

Front cover image: Device under light microscope, Future CS Hub laboratories.

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Welcome message

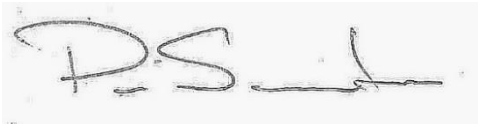
The CS Hub (http://compoundsemiconductorhub.org/; @FutureCSHub) has had an exciting 2018, working towards our goal of ***establishing the UK as the global centre for CS research and manufacturing***.

We have developed the CS Cluster (http://www.csfusion.org/) with our partners, a venture which connects CS manufacturing from research to product, and from wafers to systems. The team has pushed forward science supporting 5G communications and imaging, including establishing basic RF GaN-Si HFET technology, developing new patented growth of µLED arrays and excellent progress on magnetic imaging systems.

We have delivered professional development training on Photonics and GaN Electronics Technology to industry. Investment has improved our facilities, and we have welcomed 13 new industrial partners during 2018.

Over the next year we will push forward the performance of compound semiconductor electronic and photonic structures grown on Si and develop additional links with industry partners. Research will include development of fast-fab (for rapid feedback on CS device performance) and GaN MMIC processes, optoelectronic devices for harsh environments and high performance IR detectors for use in applications such as surveillance.

Prof Peter Smowton, CS Hub Director and Head of School of Physics and Astronomy, Cardiff University



Prof Peter Smowton
CS Hub Director,
Head of School,
School of Physics &
Astronomy,
Cardiff University

Introduction

As part of an effort to evolve critical mass investments in manufacturing, and develop research associated with significant manufacturing challenges, EPSRC, together with industry, have supported eight Future Manufacturing Hubs. As one of these Hubs, the Future Compound Semiconductor Manufacturing Hub (CS Hub) addresses the need to integrate compound semiconductor and Silicon manufacturing, applying the manufacturing advances made in one type of compound semiconductor across the different families of compound semiconductors, and combines these different compound semiconductors for optimum functionality.

Compound semiconductor materials, and increase in manufacture of compound semiconductors, are Key Enabling Technologies essential to next generation technologies at the heart of modern society.

The CS Hub has 3 key outcomes :

- To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
- To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
- To generate novel integrated functionality such as sensing, data processing and communication.

Made up of a core Hub at Cardiff University, the CS Hub has spokes at the University of Manchester, the University of Sheffield and University College London (making up the original academic CS Hub partners) as well as 24 original industrial backers.

The CS Hub forms an integral part of the CS Cluster based in South Wales, the first of it's kind in the world. The CSCluster forms a complete manufacturing chain from Translational Research Level (TRL) 1 to 9 and currently comprises 9 collaborating partners. The CS Hub makes use of the world leading facilities and expertise at the Institute for Compound Semiconductors (ICS, Cardiff University) and feeds the higher TRL 4+ activity at the Compound Semiconductor Centre (CSC) which links to the UK manufacturing industry and the Compound Semiconductor Catapult. The CS Hub is resourced to research and develop new manufacturing processes, leveraging existing capital investment and completing the Welsh Government strategy to generate a major UK CS Cluster.

Compound semiconductors are essential for the development of:

- 5G
- energy efficient lighting
- smart devices
- electric vehicles
- imaging techniques.

Compound semiconductors are vital to development of technologies supporting:

- a connected world
- health
- security
- the environment

The Hub will:

- position the UK at the centre of CS manufacturing research.
- support & promote CS research and systems research in all associated fields.
- apply the manufacturing disciplines and approaches used with Silicon semiconductors
- combine CS with Silicon to generate the required increase in CS manufacture.

Structure

Internal Structures & Regulation

Summary Statement

Our Hub of CS research activity and operational headquarters is located at Cardiff University, led by CS Hub Director, Professor Peter Smowton. This central entity interacts highly with three spoke universities: University of Manchester, University of Sheffield and University College London, as well as a large number of industrial partners and collaborators.

The CS Hub structure includes a Management Board and Strategic Advisory Board as well as support structures for each of eight work packages and two grand challenges.

Management Board

The Management Board reports to the CS Hub Director and is comprised of a number of senior Hub members who are able to represent fully the research interests of the Hub. All members meet quarterly to discuss and plan the research of the CS Hub.

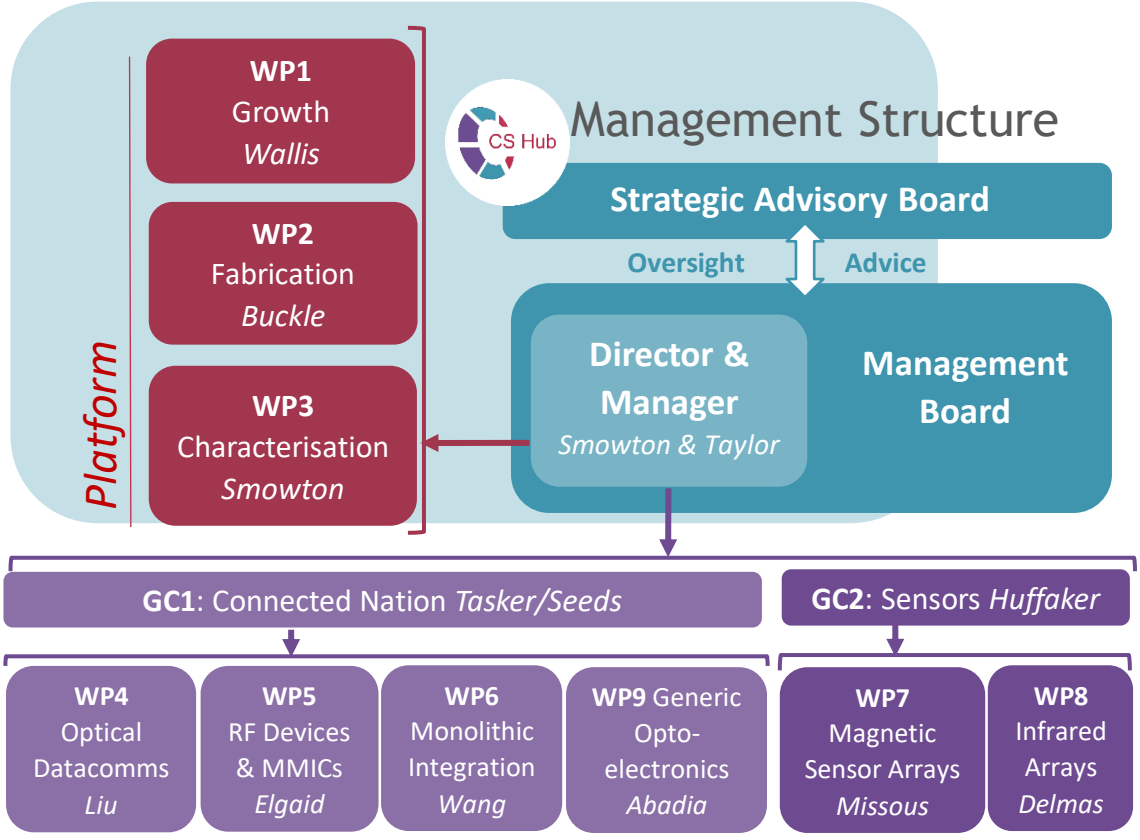
Strategic Advisory Board

The Strategic Advisory Board provide guidance to the CS Hub Management via a biannual meeting. The Board includes world leading research and industry experts in the field of compound semiconductors.

Strategic Advisory Board meetings provide an opportunity for Hub members to receive guidance and direction from impartial, highly experienced and knowledgeable individuals.

Work Package Governance

Originally the CS Hub was divided into eight research areas: 3 Platform Work Packages which spanned across 4 "Connected Nation" Grand Challenge Work Packages, and 2 "Sensors" Grand Challenge Work Packages. This year we have added an additional work package to the Connected Nation Grand Challenge. This new Work Package 9 will be described later.



The CS Hub Management Structure. The Director is advised by a Management and Strategic Advisory Board. Platform Work Packages 1-3 underpin 2 Grand Challenges made up of 6 further Work Packages.

Membership of the CS Hub management structures is shown in the tables. The Hub is governed by a Management Board made up of senior members of the Hub team across the four original academic partner institutions. The Strategic Advisory Board is made up of experts from academic and industry who are well equipped to advise the Hub on research direction, identifying commercially valuable research and advising on impact paths. Our work package and grand challenge leads direct and coordinate the research of the Hub.

Management Board Members

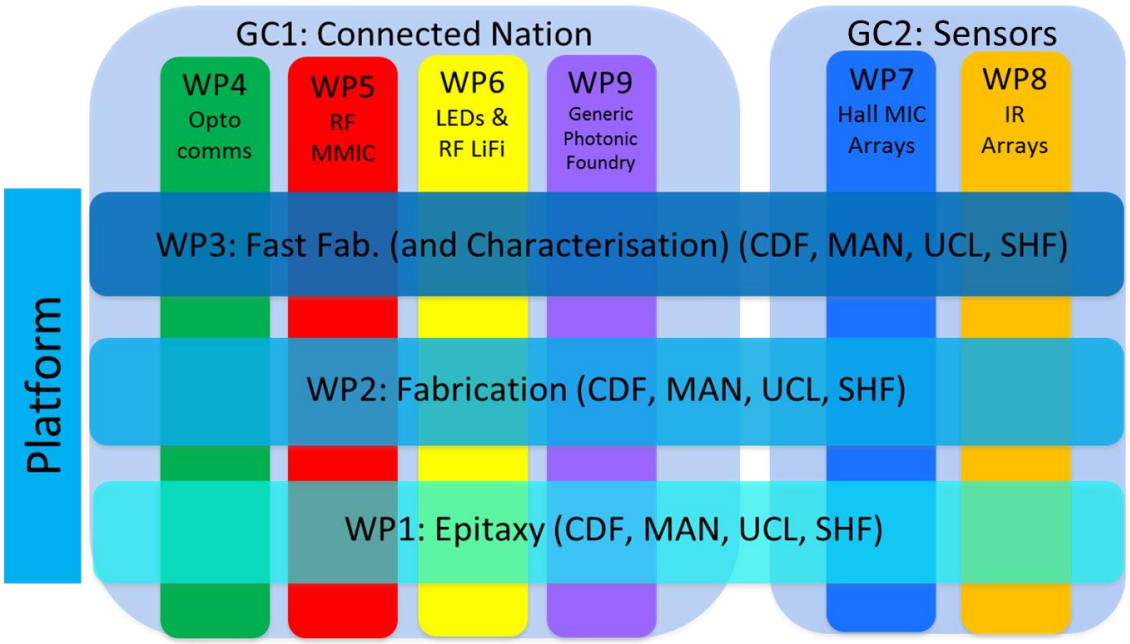
Name	Organisation
Diana Huffaker	Cardiff University
Peter Smowton	Cardiff University
Paul Tasker	Cardiff University
Wyn Meredith	CSC
Huiyun Liu	University College London
Mo Missous	University of Manchester
Tao Wang	University of Sheffield

Strategic Advisory Board Members

Name	Organisation
Richard Penty	Cambridge University
John Bagshaw	Independent Technology Consultant
Richard Bailey	EPSRC
Gerald Buller	Heriot-Watt University
Dominique Schreurs	KU Leuven
Andy Sellars	CSA Catapult
Mike Wale	TUI Eindhoven

Work Package and Grand Challenge Leads

Name	Organisation	WP Lead
Paul Tasker	Cardiff University	TL GC1
Diana Huffaker	Cardiff University	TL GC2
David Wallis	Cardiff University	WP1 Lead
Philip Buckle	Cardiff University	WP2 Lead
Peter Smowton	Cardiff University	WP3 Lead
Huiyun Liu	University College London	WP4 Lead
Khaled Elgaid	Cardiff University	WP5 Lead
Tao Wang	University of Sheffield	WP6 Lead
Mo Missous	University of Manchester	WP7 Lead
Marie Delmas	Cardiff University	WP8 Lead
Nicolas Abadia	Cardiff University	WP9 Lead

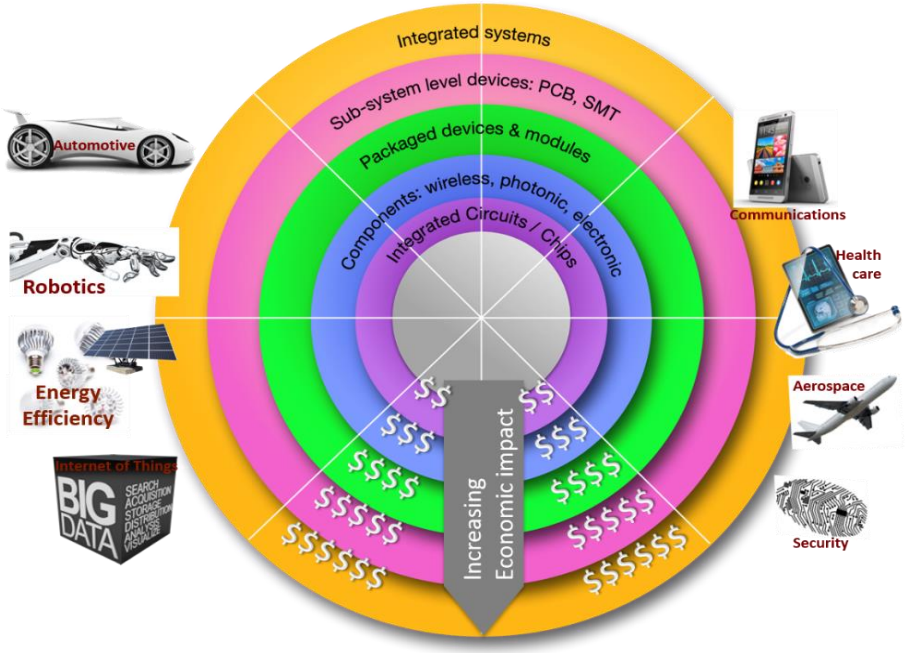


Work Package structure of the CS Hub. Two grand challenges are split into 6 areas of work, spenned by 3 "platform" areas that tie together work in the underlying work packages.

Next generation technologies will only be achieved with a huge increase in compound semiconductor manufacture.

Compound semiconductor materials are a Key Enabling Technology at the heart of modern society.

Key Outcomes:
To radically boost the uptake and application of CS technology by applying the manufacturing approaches of Silicon to CS
To exploit the highly advantageous electronic, magnetic, optical and power handling properties of CS while utilising the cost and scaling advantage of Silicon technology where best suited
To generate novel integrated functionality such as sensing, data processing and communication.



The diagram indicates the likely impact areas of technology developed via the CS Hub and emphasises the added value at each stage enabled by the CS technology.

Research landscape

CS Cluster Developments

The Future CS Hub remains an active and founding member of the CS Cluster in South Wales. CSconnected is now the formal gateway to the cluster which represents organisations directly associated with research, development, innovation and manufacturing of compound semiconductor related technologies, as well as organisations along the supply chains whose products and services are enabled by compound semiconductors.

Other members of CSconnected include core partners, the Institute for Compound Semiconductors (ICS, Cardiff University), the Compound Semiconductor Centre (CSC), the Compound Semiconductor Applications Catapult and the Centre for Integrative Semiconductor Materials (CISM, Swansea University). These are joined by business partners IQE plc, SPTS, Microsemi (Microchip), and Newport Wafer Fab.
Together we complete the supply chain for brining new CS discoveries to market. The development of the CSconnected brings us closer to achieving our mission of
"*establishing the UK as the primary global CS research and manufacturing hub*"
UKRI Strength in Places

CSconnected received early stage funding from the UKRI Strength in Places Fund for project designed to drive substantial economic growth. Submission of our full bid will take place in late 2019, with a successful outcome consolidating CSconnected and bringing significant economic benefit for the South Wales area through high value job creation and regional growth.

CCR City Deal
Significant investment (£38.5m) from the Cardiff Capital Region (CCR) City Deal has enabled cluster members, IQE plc to develop a new high-tech facility in Newport. This has generated employment for 32 highly skilled technicians, with 10 further vacancies still to be filled.

CS Applications Catapult Innovation Centre
The Catapult has received £50m in order to develop an impressive innovation centre housing a design studio, laboratories and test facilities, supported by simulation and modelling tools and advanced capabilities. The Centre aims to help companies accelerate the development of new products using compound semiconductors. The Centre will bring around 90 jobs to the area and will be based near the new IQE high tech facility in Newport, South Wales.

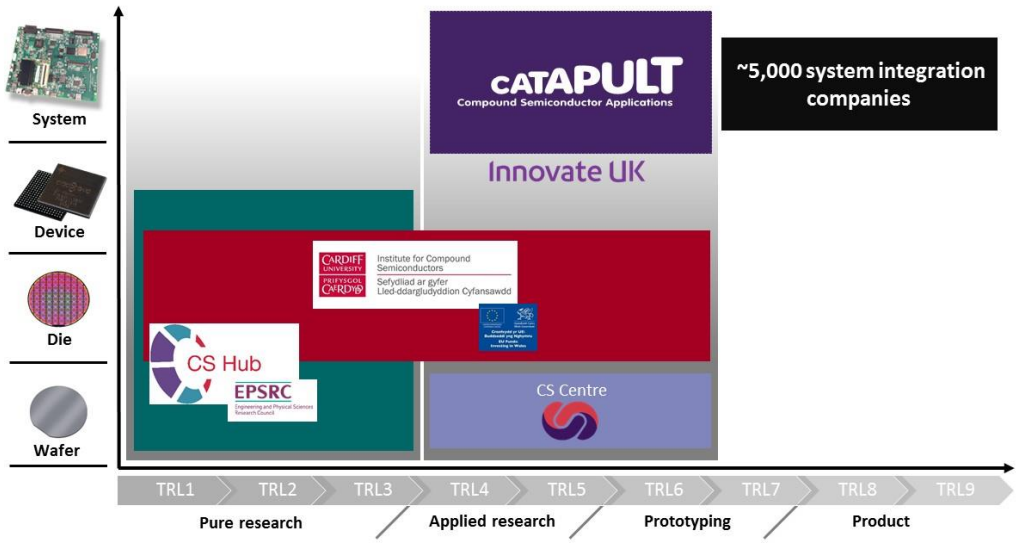


Image adapted from CS Catapult material. The CS Hub covers TRL levels 1 to 4 and works together with ICS, the CS Centre and the CS Catapult, together with several other partners, to form the CS Cluster.

Impact

How will the CS Hub Affect the Future of Manufacturing Research

Societal

Compound Semiconductor materials are a Key Enabling Technology underpinning the operation of the Internet and enabling emerging megatrends such as Smart Phone usage, satellite communications/GPS, Direct Broadcast TV, energy efficient lighting, efficient solar power generation, advanced healthcare and ground breaking biotechnology. Simply put these technologies support our connected world and the future health of the planet.

Knowledge Dissemination

We are active in dissemination of knowledge via conferences such as UK Semiconductors and Photonics West, the latter providing an excellent mix of science and commercial activity. We will publish in open access peer reviewed journals such as those from both the Nature and IEEE stables.

Our aim throughout is to engage new partners and we will hold workshops, use feasibility funding, actively canvas and make use of our existing partners and contacts, relevant KTNs, the Welsh Optoelectronics Forum and other appropriate bodies to connect as widely as possible.

Skills Base

The cutting edge equipment operated as part of a manufacturing process offers an excellent training opportunity, inculcating a manufacturing mind set in a UK strategically relevant high technology field. We will embed technological excellence and the latest manufacturing approaches in UK industry. PDRAs and students will participate in high level meetings with the commercial organisations and will work alongside R&D staff from industry. There will also be a direct economic impact via the provision of skilled workers to relevant companies, a feature of our previous projects.

Outreach

The Hub funded outreach specialist will promote the reach and importance of compound semiconductors and the strategy and activity of the Hub in manufacturing. The specialist and the team will address audiences from school students to stakeholders to politicians. Resources are available from the Hub to train researchers and staff in media interactions and outreach using a range of innovative formats such as performance and theatre production skills.

Economic

Our vision is to ensure that the UK's research strength in compound semiconductors will be embedded in manufacturable approaches so the UK can commercially address the opportunities that compound semiconductors will provide. The global market for compound semiconductors is currently worth around $33.7Bn, with a compound annual growth rate of 17.3%, and underpins 100s of billions dollar related industries from telecom to automotive. Expanding commercial activity in the compound semiconductor sector will provide an important boost for the UK economy and maintain UK advanced manufacturing competiveness. A good example of this is Cardiff headquartered IQE Plc, the global leader in supplying compound semiconductor materials (—£155M turnover, 2017 results).

Our aim is to strengthen the relationship between academia and industry and this will be achieved by 1) changing the mind set of researchers to start from solutions that allow rapid translation to production by providing access to production scale and research tools that are functionally similar along with highly skilled support for the tools and processes; 2) Co-location of research and industry staff to maximise cross fertilisation of ideas, techniques and approach in an environment that supports interaction.

The EPSRC Manufacturing Hub funded translation / business developer together with staff from the Compound Semiconductor Centre will support SMEs through product prototyping, IP generation, skills development and training. They will help bid for external grants, coordinate partner forums, form networks and prepare roadmaps.

Translation

Industry / User / Innovation Chain Engagement

In 2014 the Sheffield led EPSRC III-V centre CS roadmap identified a concern that the UK CS community was missing an exploitation link to help provide a route to impact and exploitation. Many technological solutions work well in the research environment but fail to succeed commercially. The Hub directly addresses this issue, by working to change the academic community mind set, to inspire researchers, via training and environmental changes, so they begin with solutions that allow rapid translation.

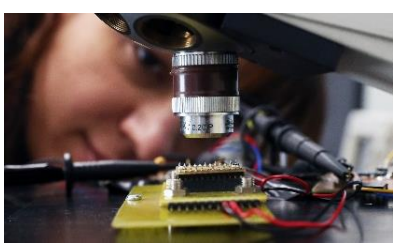
The hub is encouraging the Co-location of research and industry staff to maximise interactions. Our Grand Challenges are specifically designed to produce intermediate outputs that can be used to demonstrate the potential for successful translation.

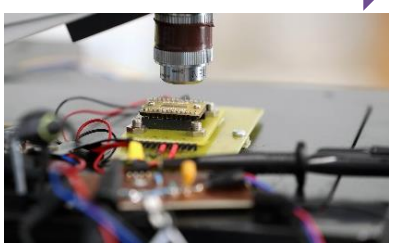
In order to promote this activity across the wider UK community the Hub has £1m to invest in new research projects. We have invested in a first round of 6x initial short-term <£40k studies, with priority given to those applications including new Hub partners. Funded studies will have a high probability of translatable manufacturable research, and will be expected to cascade into subsequent larger studies with an emphasis on translating technology from research to industry. We recognise that SME engagement is a critical element in promoting rapid exploitation opportunities and interact with a number of these.

CS Connected: User interface, represents cluster members including those below.

Future Compound Semiconductor Manufacturing Hub	**Institute for Compound Semiconductors**	**Compound Semiconductor Centre**	**Compound Semiconductor Applications Catapult**
CS Manufacturing Research	Facilities; Equipment; Services (skilled workers)	Develop and prototype CS materials	Help industry in developing novel CS materials/topology/devices
Enable high value & productivity in CS manufacturing	Research	Enable a wide range of applications	Develop systems for end-user **applications**
Building on ICS research	Product development to prototyping	Transfer R&D to product & process innovation to high value large scale **manufacturing**	
Training; Outreach	Industrial collaboration		

- **Technology Readiness Levels** **+**





Images show device development by a Hub PhD student, Cardiff University.

Comments from industry partners

Dr Wyn Meredith, Director of The Compound Semiconductor Centre commented:

"The primary aim of our business is the commercialisation of novel compound semiconductor materials technologies. Our involvement in the Hub has dramatically extended our capability reach to include novel methods of device structure design, testing and evaluation. This has resulted in Hub the and the Centre securing collaborative research, development and innovation activities worth £12M since our relationship started in 2016. All of these activities are focussed on engaging an extended UK supply chain, many of whom have never been involved in CS technologies."

Drew Nelson, Founder and CEO of IQE Plc commented:

"Our long term vision of building a regional Cluster of excellence around advanced semiconductor technologies has been significantly enhanced by the participation of EPSRC and the research community via the CS Manufacturing Hub. Since 2016, commitment has been secured in excess of £600M capital and revenue investment in the Cluster, at a rate of 5:1 private to public. The Hub is at the centre of a co-ordinated ecosystem of manufacturing innovation which is influencing the security of ~1500 high value add semiconductor manufacturing jobs in the region, which we aim to grow to 4000-5000 by 2023. To achieve this we are delivering co-ordinated action between academia, industry, local, regional and national government at an unprecedented level."

Sam Evans Director of External Affairs @Newport Wafer fab said:

''The CS Hub will provide a pipeline a new technologies and talent for the Compound Semiconductor cluster. This University technology alliance will focus the capabilities of Four leading UK Universities, Manchester, Sheffield, UCL and Cardiff. The CS Hub will utilise the resources of a major cleanroom investment at ICS Cardiff in combination with extensive knowledge and manufacturing expertise of the CS Connected companies (NWF, IQE, SPTS & Microchip). Working with the CS Hub, Newport Wafer fab will establish the next generation CS Technologies. This combined resource will bridge the TRL valley of death, developing CS manufacturing to deliver next gen CS technologies while providing a pipeline of future UK CS Technologists for the Cluster."

Dr Andy G Sellars, CS Catapult commented:

"The EPSRC Future Compound Semiconductor Manufacturing Hub, hosted at Cardiff University, has made a strong impression since it was established in 2016. The Hub is working on an interesting number of projects that are aligned to the needs of industry in the near term, and other projects that have longer term goals – providing a degree of resilience to the Hub's activities. There is good evidence the Hub is capitalising on the combined expertise from Cardiff University, Manchester University, Sheffield University and University College London. In addition, the Hub has made excellent routes to commercialisation by working with industrial partners in the compound semiconductor cluster, such as Newport wafer Fab, and other research institutes, such as the Catapult. The Hub has shown demonstrative market pull working with large industrial companies from across the UK.

Some projects are particularly impressive, spanning the research spectrum from cutting edge ideas to market acceptance, and spanning the supply chain from semiconductor materials to sub-systems. Of particular note, the advanced quantum well hall effect sensor project spun-out of Manchester University shows great market potential."

Additional expertise

CS Hub expertise

The CS Hub investigators and associated groups have been carefully selected for their track record in innovation and impact, complementary technical capability and the individual skill sets that can combine to create new solutions to the identified major scientific challenges in manufacturing.

Expertise in epitaxial growth, including growth on non-native substrates is provided by Huffaker, Li, Liu, Missous, Wallis, Wang and Wu. Buckle, Elgaid and Missous bring experience of wafer scale-up and manufacturing uniformity over these larger wafer sizes. Abadia, Beggs, Quaglia, Smowton and Tasker bring world leading expertise in design, integration and characterisation.

In addition to the Hub's Work Package Leads, we work with a number of world-leading academics to develop the highest impact research possible under the remit of the Hub.

Diana Huffaker (Cardiff University) (h-index 47) is the Welsh Government Ser Cymru Chair in Advanced Materials and Engineering and is a Director of ICS. She has made major contributions in compound semiconductor material and devices and, of particular relevance, in the growth of Compound Semiconductors on mismatched substrates including Silicon. Her current research interests include the directed and self-assembled nanostructure solid state epitaxy and optoelectronic devices including infrared detector arrays, solar cells and III-V/ Si photonics.

Michael Pepper FRS, FREng (UCL) (h-index 55, 8 patents) is Pender Professor of Nanoelectronics and has received the Royal Society's Bakerian Prize Lectureship, Hughes and Royal Medals. He is co-founder and Scientific Director of THz technology spin-off company TeraView. He is a former member of General Board and Council of Cambridge University and Council for Industry and Higher Education.

Alwyn Seeds FREng, FIEEE (UCL) is Professor of Optoelectronics. He pioneered the research area of microwave photonics and was awarded the Gabor Medal and Prize of the Institute of Physics in 2012. He is an inventor on 16 patents and is co-founder of Zinwave Ltd, which is now the third largest supplier of wireless over fibre systems in the world and was acquired by McWane Technologies Inc. in 2014.

These staff are supported by academics Rick Smith & EPSRC Manufacturing Fellow Jon Willmott (Sheffield), Max Migliorato (Manchester), Sudha Mokkapati (Cardiff) and Senior Research Fellows Siming Chen (UCL), Marie Delmas and Sang Soon Oh (Cardiff) covering design, nitride fabrication, and characterisation and growth of CS on Si.

Wafer loading onto ellipsometer in the Institute for Compound Semiconductors (ICS) clean room, Cardiff University. The ellipsometer was purchased using the CS Hub underpinning equipment award from EPSRC.

New expertise at the Hub

Evolving the expertise available at the Future CS Hub

The CS Hub has worked flexibly to ensure that our research remains highly relevant in the constantly evolving CS manufacturing environment. We have welcomed several new people to the team, bringing with them a variety of expertise essential to keep the Hub at the very peak of research excellence. We have welcomed new expertise to the CS Hub during year 2. In order to develop our research programme to ensure we deliver the best value at the highest level, we have revised our core structure to accommodate an additional work package. This work package develops work previously included under the platform work package 3 (Fast-Fab), in a new work package 9. This work is now lead by the new Cardiff University lecturer, Dr Nicolas Abadia.

In addition to Nicolas Abadia, the CS Hub has recruited several new members to our team over the past year.

Prof Khaled Elgaid has taken over leadership of Work Package 5 (Advanced RF Devices and MMICs) from Prof Paul Tasker. Paul remains Grand Challenge 1, The Connected Nation, lead. The arrival of Khaled has enabled the consolidation of technology development for RF devices and MMICs under one leadership, and we have seen excellent progress on this in particular this year.

Dr Qiang Li has also joined the Hub team at Cardiff University as a lecturer with a focus on lattice-mismatched hetero-epitaxy of III-V compound semiconductors on silicon for electronic and photonic applications. His expertise is in metal-organic chemical vapour deposition (MOCVD), selective-area hetero-epitaxy and heterogeneous device integration. Dr. Qiang Li will manage MOCVD operation and conduct the III-V on Si work for Work Package 1 and Work Package 4.

The Cardiff lab team have also been joined by a new post-doctoral research associate, Sara-Jayne Gillgrass and a new technician, Josie Nabialek. Alice Hopkinson also joins the team at Cardiff University in a Communications and Engagements role.

New CS Hub associated PhD students in Cardiff include Fwoziah Albeladi, Curtis Hentschel and Ben Maglio.
Fwoziah will be developing a narrow linewidth semiconductor laser by using generic monolithically integrated technology for use in a high optical communication system.
Curtis will be working on the design and characterization of narrow linewidth VCSELs.
Ben joins the team via an Airbus sponsored studentship, working on computational modelling and simulation of III-V semiconductor devices for design optimization prior to manufacture, fabrication and characterization.

New CS Hub Members from top: Dr Qiang Li brings MOCVD expertise; Prof Khaled Elgaid brings a wealth of experience in advanced RF devices and MMICs.

Use of flexible funding: new WP9

Generic photonic foundry

The primary structure of the Hub, comprised of underpinning Work Packages supporting Grand Challenges remains unaltered. However, to accelerate progress in topics of strategic importance, and at the recommendation of our Strategic Advisory Board, we have revised our core structure to accommodate an additional Work Package and recruited new expertise to the CS Hub during year 3.

This Work Package develops technology previously included under the Platform Work Package 3 (Fast-Fab), in a new Work Package 9 (WP9) entitled 'Generic Photonic Integration' led by new Cardiff University Lecturer, Dr Abadía.

Work Package 9: Generic Photonic Integration

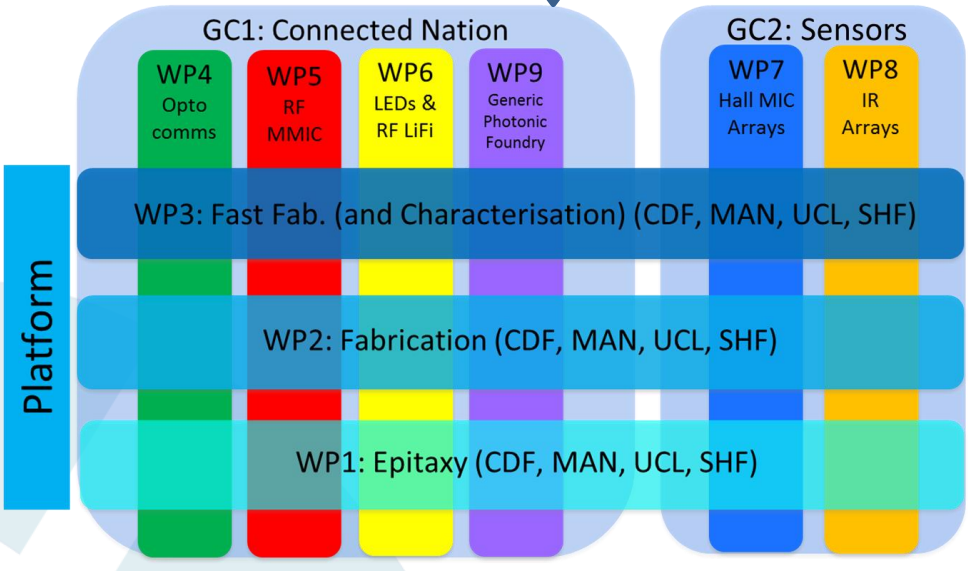
Dr Abadía, Work Package 9 lead

Work Package 9 will be comprised of generic photonic integration work on proof-of-concept of optoelectronic devices and systems. The initial driver for this technology is the provision of GaAs-based integrated optoelectronic devices and systems for interconnects used in aerospace and nuclear sectors and ultimately for telecommunication networks.

This project is led by Dr Nicolás Abadía from Cardiff University (abadian@cardiff.ac.uk) and it is done in collaboration with:

Academic partners: Cardiff University – Prof David Wallis, Prof Paul Tasker, Dr Sudha Mokkapati, Dr Roberto Quaglia; University College London - Prof Huiyun Liu; the University of Sheffield – Prof Tao Wang; the University of Manchester - Prof Mo Missous.

Industrial partners: IQE, Newport Wafer Fab, Compound Semiconductor Centre, Airbus and National Physical Laboratory.



CS Hub structure showing the location of the new WP9: Generic **Photonic** Integration, which is lead by Dr Abadía, Cardiff University.

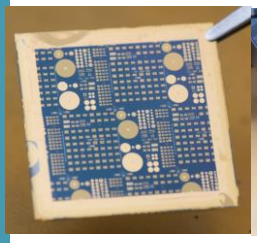
Industrial and academic partners

Generic Photonic Integration: The next generation

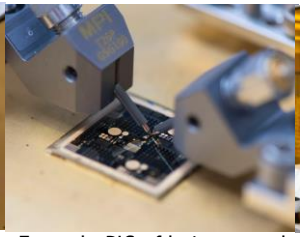
Generic Photonic Integration is a platform that allows the production of photonic integrated circuits (PIC). PICs are similar to the electronic integrated circuits used in computers and other electronic devices. The main difference between the photonic integrated circuit and the electronic integrated circuit is that the former works with light and the latter works with electricity.

The invention of the integrated electronic circuit in United States in 1958 revolutionized electronics and our daily lives. The field progressed very quickly from very basic old computers used in big research facilities to a wide range of systems used in our daily life: mobile phones, tablets, laptops, WiFi and the Internet, etc. In a similar way, PICs will revolutionize several fields including next generation telecommunication networks like the Internet or the mobile network.

PICs can drastically increase the capacity and reduce the cost and power consumption of networks. This will allow the streaming of 4K content to your computer and smart TV or the development of the next generation mobile network (known as 5G) which will allow the implementation of new services like the self-driving car, telesurgery or portable virtual reality.



Example of PIC



Example PIC of being tested

Example of fabrication equipment at Cardiff University

WP9 Progress so Far:

We have started this work package by designing devices and systems to be used in the aerospace, nuclear and telecommunication sectors. We are also building a state-of-the-art infrastructure at Cardiff University to test the devices and systems we fabricate to meet industrial quality standards.

We are working with several industrial partners in Wales and the rest of the UK to identify other needs in our economy to improve its competitiveness. Among others, we are collaborating with IQE, Newport Wafer Fab, Compound Semiconductor Centre, Airbus and National Physical Laboratory; and other universities including University College London, the Manchester University, and the University of Sheffield.

Several examples of testing equipment at Cardiff University

WP9 consists of different stages:

- Design phase: we design devices and systems that will drive next generation networks.
- Fabrication phase: fabrication of the devices and systems in a reliable and cost-effective way.
- Testing: we test the fabricated designs to assure they meet industrial quality standards.

Meet the team:

Dr David Hayes

Dr Emmanuel Le Boulbar

Benjamin Maglio

Platform work package 1

Materials Growth (Epitaxy)

Summary
The main scientific challenges for epitaxial growth involve the formation of high quality compound semiconductors on silicon, including the development of semipolar GaN on Si, and the growth of mismatched InAs / GaSb on GaAs.

Lead: David Wallis WallisD1@Cardiff.ac.uk

Contributing academics for work package 1 (WP1) include Tao Wang (Sheffield), Mo Missous (Manchester), Huiyun Liu (UCL), Qiang Li (Cardiff) and Marie Delmas (Cardiff). Project partners are the Future CS Hub sponsored feasibility studies: "Three dimensional mapping of active compound semiconductor structures" and "Feasibility of compound semiconductor non-volatile RAM manufacturing on Si substrates".

WP1 encompasses all the epitaxy activities that are relevant to the CS Hub. These include non and semipolar GaN growth for optoelectronics, III-As for photonic integration, metamorphic structures on GaAs for magnetic sensors and arsenides and phosphides for optical devices.

A large amount of our work is performed on the growth of III-Vs on Si. Sharing of expertise among work package participants is a vital part of this platform work package, and excellent communication across the other work packages is allowing the rapid development of solutions to growth issues, and improved material quality.

We have developed a set of materials targets across all materials platforms and a thorough benchmarking procedure to ensure the relevance of these targets. Benchmarking targets have been developed which are dictated by the device performance required to deliver the goals of the Grand Challenges. In many cases these are internationally leading.

Major challenges with WP1 have consisted of the reliability of our growth reactors. We are using alternatives and outsourcing as needed to remain on target. For example, we are working with University of California Los Angeles (UCLA) to deliver MBE, and purchasing phosphide templates from Cea-Letti. Our fortnightly conference call for this work package is extremely important as a platform for sharing best practice and knowledge.

Progress and achievements

D1/D5 GaN based optoelectronic materials
Work has focused on the optimisation of HEMT structures on non- and semi-polar GaN. Modulation doping and delta doping have been investigated. Further studies have looked at increasing carrier concentration by increasing doping concentration and increasing the thickness of the doping layer.

D2/D3 III-As based photonic integration technology
Growth of several high density Q-dot samples was completed. We have had a new high temperature (1200oC) manipulator fitted to our MBE reactor to allow increased functionality.
Our MOCVD system is now producing good morphology, uniformity and yield of Q-wires. We are working with Bath University to develop patterning of Si substartes for growth of structures. The development of KOH etching is ongoing.
Sb materials continue to be sourced from UCLA and good progress has been made towards delivering the device structures.

Platform work package 2

Fabrication

Summary
Here the emphasis is on developing fabrication processes on up to 200mm wafers, where possible, compatible across different materials and devices.

Lead: Phil Buckle BucklePD@Cardiff.ac.uk

Contributing academics for work package 2 (WP2) include Mo Missous (Manchester). Project partners are the Institute for Compound Semiconductors (ICS), Cardiff University

WP2 has been redefined (due to changes in other work packages and consolidation of technologies under WP5) to now include only the development of passives for MMIC implementation. We have successfully probed and characterised small area test samples. Fabrication of 6" wafers is underway. We aim to deliver fully characterised designs for passive components on GaN at large wafer scale (6") by the end of 2019.

Passive fabrication translated from Manchester has been re-designed to allow dielectric etch back rather than a conventional III-V lift off process. This becomes a more industrially compatible process with potentially higher yield and enables much higher deposition temperatures to be used for the dielectric, without any added complexity to the photolithography step. This should enable higher quality and more uniform capacitance structures to be available whilst reducing process steps. Currently wide area metal deposition uniformity is being assessed utilising the adopted statistical gathering and analysis software (JMP - 'JuMP'),
New 6" wafer maskset is now procured, replicating the Manchester passive library for test. First process ran after characterisation of Ni:Cr sputter target complete.

Once we have an initial testbed on 6", we will engage with RF design companies to steer performance data, and international benchmarking. Success will be measured by large area wafer yields and circuit yields, preceded by device yields for devices within individual workpackages.

Areas of focus over the next period include full characterization of 6" GaAs wafer passives (cross testing with Manchester); Opening discussion with external design houses for acceptable statistical data requirement (for desirable MMIC design); Transfer to GaN samples/wafers and transfer/integration with GaN FET programme (WP5).

Our major challenge is a lack of 8" capability, and no suitable in house dielectric, however we are progressing with 6" capability and utilizing collaboration with Swansea University.

Progress and achievements

Significant progress has been made on passive development. The maskset has been tested and process flow established on small area (2 cm x 2 cm) GaAs tiles. New resist processes have been run up using single layer resists suitable for lift off to enable efficient (and cheaper) future fabrication, without the need for bi-layer, or post deposition treatment (e.g. electrochemical plating to increase metal thickness, or ultrasonic treatment to achieve lift off). Where possible reductive processes have been used.

A full process run using newly commissioned fully 6" capable toolset has been completed and is awaiting autoprobing to test (benchmark) structures against intended device design. If successful, these will be sent for 'round robin' measurement to cross reference both processing and characterisation consistency.

New funding was brought in via the WEFO supported ACNM project. This will contribute the the manpower required to deliver passives for WP2.

Platform work package 3

Fast fab and characterisation

Summary
The main scientific challenges include the scaling up of characterisation approaches including developing on-wafer testing and the development of fast fab approaches to minimise the growth, fabrication, characterisation development cycle time.

Lead: P Smowton
SmowtonPM@Cardiff.ac.uk

Contributing academics for work package 3 (WP3) include Nicolas Abadia (Cardiff), Phil Buckle (Cardiff), Khaled Elgaid (Cardiff), Huiyun Liu (UCL), Mo Missous (Manchester), Mokkapati (Cardiff), Quaglia (Cardiff) and Rick Smith (Sheffield). Project partners are IQE, Huawei, NPL, CSC, CST, ICS ltd.

Overarching themes for WP3 are approaches to provide rapid feedback to epitaxial growth and fabrication as well as reliability studies. Latest results indicate mechanisms involved in the degradation of quantum dot lasers on Silicon and the means to mitigate them. These are being incorporated within our device design. Our approaches should be sufficiently fast to be incorporated within a normal growth or fabrication cycle and sufficiently detailed to provide meaningful information.

International benchmarking is tied to performance of devices that these approaches support. Such as the reliability of lasers grown on Silicon (carried out under WP4) and the improvement in performance resulting from growth fabrication characterisation iterations .

Our major challenge is to operate at the scale and volume required to establish statistically relevant results. To address this we are scaling up measurement capability, devising experiments to determine mechanisms more directly to reduce reliance on large numbers.

Progress and achievements

We are working on upgrading reliability facilities for ramp up of testing. For example, the heater system for maintaining device temperature outside the oven during intermittent testing has been upgraded. The light measurement part is under construction for completion soon.

We have evaluated our current Sharetree system, and delivered a report on the changes required to upgrade the system to allow measurements on detectors. We hope to implement the changes to enable detector measurements in the near future. We are working towards delivering a paper on VCSELs.

WP3 has expanded to include some pilot activity required for a new proposal. Due to additional resources being required, the Management Board decided to stop work on InAs dots on InP on Si for long wavelength in WP4. We hope to continue this work in a new project/proposal. We are working on preliminary data to show the feasibility of this work in WP3.

Fast fab of lasers and amplifiers has been developed for the InP based materials and results are being obtained for conference submissions and a publication on this topic to support the future proposal.

Work package 4

Manufacturing technology for optical data communications on silicon

Summary
Very recently, high-performance silicon-based InAs/GaAs quantum dot (QD) lasers have been demonstrated with CW operation at high temperature (>75 ºC) and long lifetimes (>100,000 hours). Here we will develop our world leading III-V-on-Si technology to create high performance lasers and semiconductor optical amplifiers (SOAs) for datacommunications applications.

Lead: Huiyun Liu
Huiyun.liu@ucl.ac.uk

Contributing academics for work package 4 (WP4) include Siming Chen (UCL), Qiang Li (Cardiff), Alwyn Seeds (UCL), Sam Shutts (Cardiff), Peter Smowton (Cardiff). Project partners are Oclaro, Huawei, Cea-Leti, Teraview, Rockley Photonics, III-V Lab.

We have demonstrated the ultra-low threshold optically pumped QD micro-disk laser and first QD photonic crystal laser monolithically grown on silicon. The physics behind high-performance QD laser grown on silicon has been explained. We have developed the defect filter layers, while p-doped QDs are under investigation and will be further explored in this project.

Our target specification has required the development of laser diodes with operation up to 125 °C, which has been achieved. We are also aiming for a high-gain active region with gain > 50 cm-1. Our international benchmarking exercise shows that high-gain QD materials were developed with maximum gain around 50 cm-1 on GaAs-based devices by QDLaser and on Si-based devices by UCSB. The defect density < 1 x106 cm2 in III-V buffer grown on silicon from this project is international leading.

Our major challenge is to increase the gain of the QD active region. P-type modulation doping and high QD density are under investigation. We are investigating the growth of high density QD (>5.5×1010 cm-2) with high uniformity (linewidth < 25 meV). Initial results are promising (under going).

Progress and achievements

Initial results from high-density InAs/GaAs QD lasers on GaAs are completed and further fabrication and detailed characterisation on these samples are undergoing.
Recent collaboration with Hong Kong University of China produced a demonstration of ultra-low threshold QD microdisk lasers directly grown on on-axis Si substrates. Furthermore, first QD photonic crystal laser directly grown on on-axis Si substrate has been demonstrated.
The development of InAs/GaAs quantum dots on on-axis silicon (100) substrates is on-going.

Work package 5

Advanced Radio Frequency Devices & MMICs

Summary
Building-on on-going success, in demonstrating a UK III-V-on-Si GaN based HFET technology baseline, this work package aims to ultimately establish a full III-V-on-Si HFET device and MMIC technology platform for high/medium power microwave wave system applications. We will use high-frequency device performance at staged points to allow feedback for optimisation of the epitaxial growth and device technology and encourage industrial engagement.

Lead: Khaled Elgaid ElgaidK@Cardiff.ac.uk

Contributing academics for work package 5 (WP5) include Roberto Quaglia (Cardiff) and Paul Tasker (Cardiff). Project partners are IQE, SPTS, Newport Wafer Fab, CS Catapult, MBDA, IconicRF, Leonardo, Arralis and Huawei. These contacts are involved in design and or fabriacation.

Our aim is development of the RF GaN-Si HFET device and MMIC process, supported by full characterization and design activities: CAD models for MMIC design and PDK documentation, and demonstration by some reference designs. This will require technology development for RF Device and MMICs; PDK Development for RF Device and MMIC Characterization and Modelling; MMIC Design for Quasi-MMIC GaN-Si/GaAs solutions and GaN-Si MMIC solutions.

In terms of a target specification, this will be dependent on final performance technology/design integration/interaction dependent. We will aim for 3 - 4W/mm output power, gate length ~ 250nm, Ft ~ 45GHz, power ~ 3 W/mm at 28V, efficiency is 65% at 28V, high-gain active region with gain > 50 cm-1. This target is generally achieved by other leading researchers in the field.

Progress and achievements

Basic GaN electronic devices technology development has been a major focus. Complete GaN HEMTs have been fabricated; this technology was originally developed as part of an on-going EPSRC ET project.

PDK Development: RF Device and MMIC Characterization and Modelling: Basic structures are realised. Work was carried out at the JWNC Glasgow and supported by the EPSRC ET project.

MMIC Design: Quasi-MMIC GaN-Si/GaAs RF Device and GaN-Si MMIC Solutions: Quasi-MMIC activity using a GaN-SiC/GaAS technologies from Quovo is ongoing. Assembled circuits are undergoing full RF characterisation. This activity will increase when we have WP5 devices fabricated and characterised.

Work package 6

Monolithic Integration of RGB LEDs & Integrated RF Electronics for LiFi

Summary
Building on the work in the platform our approach is to use nitrides where they can be efficient and fast enough by using semi-polar or non-polar for green and yellow combined with other CS for longer wavelengths. We will use multiple selective area growth steps to integrate CS/Si structures with several different epitaxy designs on the same substrate.

Lead: Tao Wang
t.wang@Sheffield.ac.uk

Contributing academics for work package 6 (WP6) include Huiyun Liu (UCL), Alwyn Seeds (UCL), Rick Smith (Sheffield), Peter Smowton (Cardiff), Paul Tasker (Cardiff). Project partners are Cambridge GaN Device, Plessey, IQE, SPTS, Newport Wafer Fab, CS Catapult, MBDA, IconicRF, Leonardo, Arralis and Huawei, and two CS Hub sponsored feasibility projects.

Li-Fi exhibits striking advantages compared with current Wi-Fi technology in terms of bandwidth, data transmission speed. The major component of Li-Fi is visible LEDs which need to have ultra-fast response time and need to be controlled by high frequency electronic component. Integration of III-nitrides (blue, green) and other III-Vs (red) on low cost and up-scalable silicon substrates for simultaneous general illumination and Li-Fi is the best way forward, where the LEDs transmitters can be controlled by GaN based HFETs uniquely.

We aim to develop monolithic on-chip integration of microLED and HEMTs; (1)advanced overgrowth of microLEDs; (2) initially c-plane GaN based HEMT, and then semi-/non-polar HEMTs. Our target of an integrated III-nitride LED-HEMT-(Photodiode) for ultra-fast visible light wireless communications on >1 GHz scale, currently does not exist.
Others have recently demonstrated a maximum raw data rate~86.4 Mbits/s @256 MHz) (PureLiFi). While the Hong Kong University of Science and Technology demonstrated a maximum data rate~16.7 Mbits/s by integrating III-nitride blue LEDs and HFETs on c-plane sapphire.

Our major challenges are: (1) Conventional process for microLED fabrication leads to huge damage; (2) C-plane GaN limits applications due to limited bandwidth; (3) Longer wavelength LEDs such as red are missing for III-nitrides base. To address these, WP 6 has developed a new approach to epitaxially achieving micro-LED (overgrowth on patterned substrates) in order to eliminate all the issues resulting from the conventional approach of microLED fabrication; developed a reliable approach to semi-polar GaN overgrowth on patterned silicon; will combine MOVPE and MBE to integrate III-nitrides with GaAsP (AlGaAsP)

We have learned that combined anisotropic chemical etching and photolithograph techniques for the fabrication of patterned silicon substrates is required. Selective deposition of SiO2 and wet-etching depth are two major parameters for eliminating Ga-melt back etching issues; The parameters of mask stripes, such as width, etching depth, surface treatment, are crucial. Fabrication of integration of LEDs and HEMTs needs to be properly designed in order to avoid any short circuits or open circuits. Quality control in each growth step for the new approach to microLED growth is important. Selective growth of GaAsP (AlGaAsP) by MBE is required, and a proper mask design is required.

Progress and achievements

Progress is on-going as planned; modified objectives include integrated micro-LEDs/HEMTs. Integrated micro-LEDs/HEMTs is expected to be the best option for achieving ultra-fast Li-Fi applications compared with an integrated planar emitters/HEMTs. We are the only group to achieve semi-polar (11-22) GaN with excellent uniformity and reproducibility overgrown on patterned (113) silicon. It has been identified that the delta doping approach which is very successful in previous growth of AlGaAs/GaAs HEMTs may not be useful for the growth of non-polar/semi-polar GaN HEMTs. The formation mechanism of semi-polar Gan HEMTs needs to be further investigated.

Work package 7

Magnetic Arrays

Summary
The approach is to integrate high electron mobility 2DEG with the epitaxial layer structures for all of the analogue and some of the digital electronics.

Lead: M Missous
missousm@Manchester.ac.uk

Contributing academics for work package 7 (WP7) include Max Migliorato (Manchester). Project partners are BAE Systems, Renishaw, TWI, Microchip, TataSteel, OGTC, Metropolitan Police, Home Office.

Our overarching theme for WP7 is magnetic imaging. Magnetic imaging using QWHE is a superior alternative to metal detection using coils and this is being applied in a range of industrial projects (including concealed weapon and threat detections).

Our major challenges include minimising the distance of sensor to sample (< 20 µm for micron size domain imaging); increasing sensitivity and lowering noise; Real time imaging (< 1 min for very high resolution 10x10 cm plates). In order to address these we are working on novel packaging and new field concentrators techniques; higher sensitivity materials (InGaAs-InAlAs on GaAs) and multi channel ADC data acquision.

To the best of our knowledge we are the only group using QWHE sensors for magnetic imaging. We are now in extensive electromagnetic non destructive testing (NDT) benchmarking against established Magnetic Particle Inspection (MPI), Eddy Currents (EC) and Alternating Current Field measurements (ACFM) techniques (sponsored by BAE Systems and with participation from RR and EddyFi. The QWHE imaging technique introduces new image modalities.

Our benchmarking targets include:
2DEG Targets:

- µ >6500cm2/Vs, Ns >2.5e12/cm2 and Rs< 260hm/square,
- Compressive strain(QW) less than 1.5%
- Achieved
- Surface roughness ~ 0.4nm (on Target)
- DCXRD characterisation
- Mobility= 6800 cm2/Vs (Leading)
- Ns=3.2e12 /cm2 (Leading)
- Rs-245 Ohm/square (Leading)

Progress and achievements

Our progress is on track, all basic discrete elements are fabricated and metamorphic growth of InGaAs-InAlAs on GaAs has begun. Further work will be completed on optimising stress relief buffers.
We have completed a first run of Gen 1 QWHE array fabrication and improved yield on <5 µm arrays in a second fabrication run. Our first QWHE arrays are packaged and tested.
We have established important new links via funded projects with Metropolitan Police (Threat detection using a Miniaturised MAgnetic Camera (MiniMAC) and the Oil and Gas Technology Centre (OGTC) (Corrosion Under Insulation imaging) exploiting and further developing imaging sensors for stop and search and Corrosion Under Insulation in oil pipes imaging.

Work package 8

Infra Red Arrays

Summary
The IR sensing epitaxial structures will consist of LWIR-SLS detectors grown on GaAs. WP challenges will be achieving high material quality with high uniformity, and the growth challenges associated with this. Growth conditions will be optimized, and high performance detectors will be designed before model characterisation.

Lead: Marie Delmas

Contributing academics for work package 8 (WP8) Dr Baolai Liang (University of California, Los Angeles), Dominic Kwan (Cardiff).

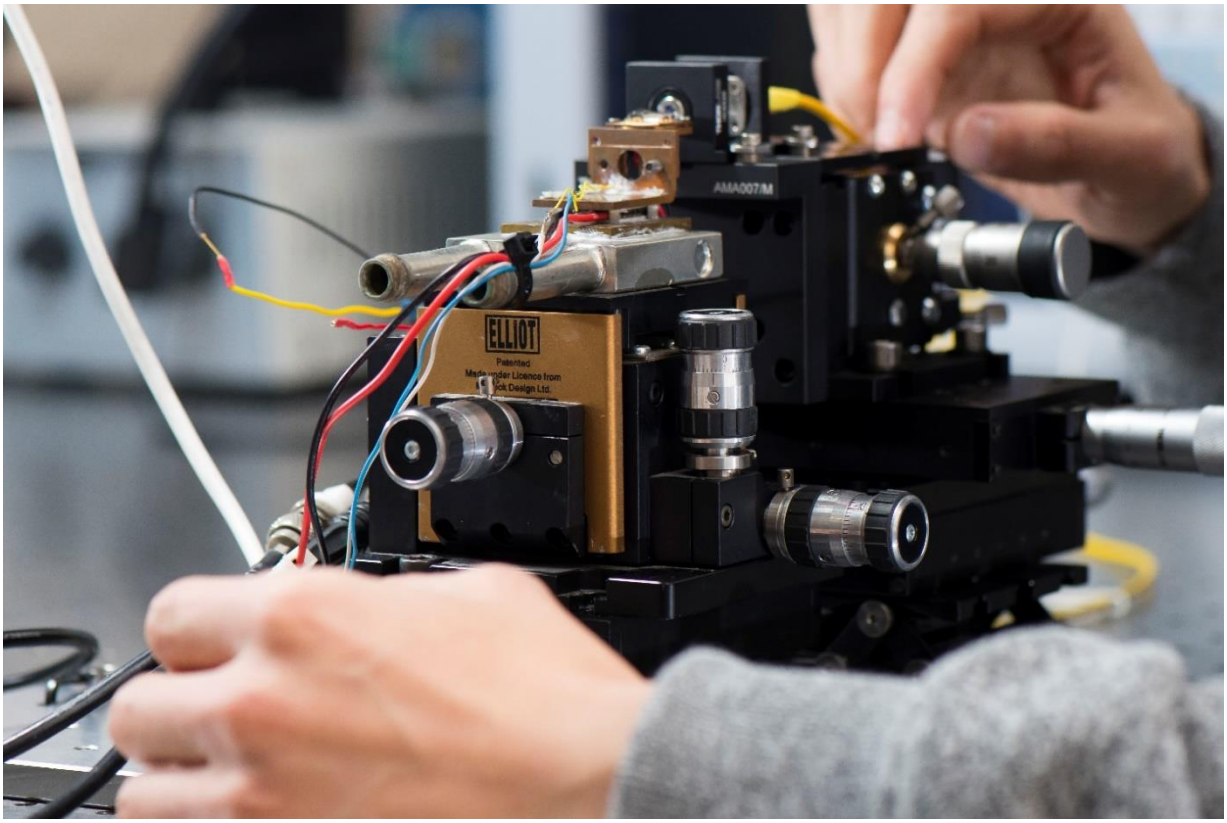
Our overarching theme is high performance infrared (IR) detectors to target specific applications such as spatial (i.e. earth observation, space object surveillance etc); Type-II InAs/GaSb superlattice (T2SL) material system for long wavelength spectral range (LWIR); Demonstration of IR array on GaAs substrate to have an impact on the overall manufacturing cost;

Major challenges for this work include, for T2SL growth by MBE: no atom in common between InAs and GaSb, lattice mismatch between GaSb and InAs (0.6%), GaSb and GaAs (7.8%). For the fabrication IR array we need to ensure a high fill factor, reduce/ suppress leakage current, process suitable for integration up to camera level. For high performances we need to ensure a low dark-current and high quantum efficiency. In order to address these challenges we have optimised the shutter sequence during growth to obtain lattice matched T2SL on GaSb substrate, this is being extended to GaAs substrate by studying growth of GaSb buffer layer on GaAs substrate. We are developing dry plasma etching via ICP using Cl2/Ar or BCl3/Ar and studying dielectric passivation. Simulation tools have been/are being developed to elucidate material properties and optimise device design.

We would like to develop device performance to target specifications of: Dark current level: J(-50mV) ~ 1-5 x 10-3 Am/cm2 for λcut=off = 10.5 μm at 77K for p-i-n device grown on GaAs substrate (expected to be lower for barrier device); Quantum efficiency: η ~ 20-30%. These targets are the typical performances of LWIR T2SL on GaSb substrate. For demonstration in single-pixel configuration on GaAs substrate, our target is state-of-the-art. For Focal Plane Array (hybrid detector array) demonstration, our target is internationally leading. To the best of our knowledge LWIR T2SL FPA never been reported in the literature.

Progress and achievements

We have delivered T2SL on GaSb by MBE and GaSb buffer layer on GaAs substrate (via IMF technique, using UCLA expertise). We are developing T2SL on GaAs substrate for single pixel detectors. XRD, AFM and PL measurements have been performed. RMS values are 5-10 times higher and PL intensity >x10 lower that for samples grown on GaSb substrate. We are working on fabrication of fabrication of T2SL single pixel detectors using MWIR wafers from Sheffield University. For the qualified model, we have delivered k.p. modelling.
LWIR T2SL on IMF on GaAs substrate samples have been grown: 2 calibration samples and 2 pin device structures. The T2SL periods are 14 ML InAs/7 ML GaSb and 12 ML InAs/4 ML GaSb.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Feasibility studies in CS research

Rounds 1, 2 and 3

During year 2, we released our first call for applications to our Feasibility Study fund. This fund, totalling £1M (full economic cost) is reserved for new studies which push the boundaries of CS research. The aim of funding these Feasibility Studies is to broaden the reach of the Future CS Hub by encouraging new academic and industry partnerships, whilst supporting new cutting edge research with complementarity and alignment with the Future CS Hub objectives.

We originally envisaged supporting up to 10 projects of average length of 7.5 months, however, we have used the flexibility available to us to set out a more extensive strategy for engaging with new partners and delivering key performance indicators via Feasibility Study funding.

Funding plan

Our first funding round, the studies funded during which have now concluded, called for applications of up to £40k (80% full economic cost) over 6 months. This is being followed with an opportunity for successful round 1 studies to apply for up to £96k (80% full economic cost), with this funding intended to lead to and facilitate a large scale EPSRC or Innovate UK grant application with strategic alignment to the Future CS Hub.

In addition, a third funding round is planned which will be coordinated with funding calls from other Future Hubs. This final call will invite new applications from areas that overlap between the Future Hub's involved, strengthening the links between Hubs and promoting interaction as well as delivering value for money.

Evaluation of applications for funding

The Future CS Hub Management Board hold responsibility for awarding funding for Feasibility Studies. The Management Board have taken the advice of the Strategic Advisory Board in assigning funding to applicants, and will continue to prioritise this advice in future evaluations.

Applications for the first round of funding were prioritised for funding according to the delivery of new academic and industrial collaborators, and were then scored on:

1. Scientific Quality and Clarity
2. Potential Impact/Opportunity
3. Hub Alignment

These criteria were used to enable new academic collaborators to request funding for new and innovative research projects which were aligned to the Future CS Hub strategy.

Funded applications

Six studies were awarded round 1 feasibility study funding, and they began their journey with the Hub on 1st August 2018 and were 6 months in duration.

We have subsequently released a funding call to enable the most promising of these studies to continue their work with us. These continuation studies will build on the successful feasibility studies and deliver additional key performance indicators for the Future CS Hub.

Introducing the 6 new Future CS Hub-funded feasibility studies

The CS Hub is investing £229,992 in 6x 6-month high-risk, novel studies. The research is aligned with CS Hub mission and vision, and will contribute to the achievement of our Key Performance Indicators.

5 New academic partners

3 New industrial partners

5 Consolidated links with existing industrial partners

£74,700 Industrial contribution

£57,498 Matched funding contribution

£132,198 Total added value

The investment and added value from the Future CS Hub sponsorship of six new Feasibility Studies in CS research.

PI	Institution	Title	Hub Mentor
Oleg Kolosov	Lancaster University	***Three-dimensional mapping of active compound semiconductor structures.***	Tao Wang
Robert Taylor	University of Oxford	***Angled-Cage Etching of Semiconductors (ACES)***	Peter Smowton
Petar Igic	Swansea University	***Solo - GaN 600V - 1.2kV Power Trench MOSFET***	Phil Buckle
Manus Hayne	Lancaster University	***Feasibility of Compound Semiconductor Non-volatile RAM Manufacture on Si Substrates***	Dave Wallis
Karol Kalna	Swansea University	***Spin Injection Into Dilute Magnetic Gallium Nitride Transistors***	Khaled Elgaid
Martin Kuball	University of Bristol	***Novel characterization techniques for GaN RF electronic epitaxy***	Paul Tasker

Details of the successful Future CS Hub Feasibility Studies funded during the round 1 funding call

Feasibility study:

Three-dimensional mapping of active compound semiconductor structures

Lead applicant: Prof Oleg Kolosov, Lancaster University
Partners: Bruker UK Ltd, Lancaster Materials Analysis Ltd.
Hub Mentor: Tao Wang

Summary

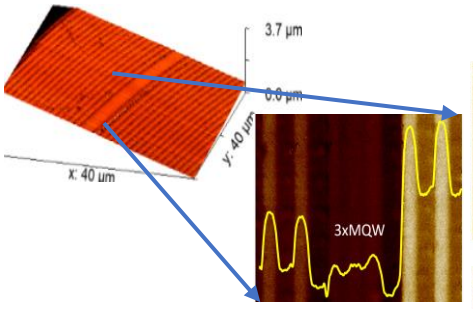
Compound semiconductors (CS) are cornerstones of modern technology – powering high efficiency GaN street lights and advancing GaAs-based devices for telecommunication. Their progress critically depends on the detailed knowledge of local physical properties of complex three-dimensional (3D) structures involved – nanometre dimension quantum wells, quantum dots and nanowires (NWs). This project created an innovative combination of 3D nano-cross-sectioning and material sensitive scanning probe microscopy to reveal nanoscale electrical, mechanical, and piezoelectric properties of buried CS nanostructures not accessible before. It resulted in world first reports of nanoscale 3D maps of surface potential in multiple quantum wells and observed polarity variation within the individual NW. These unique capabilities boost the development of CS materials by offering direct insight into the fundamental phenomena leading to the improved device performance, and providing key information to advance manufacturing processes.

Outcomes/major findings

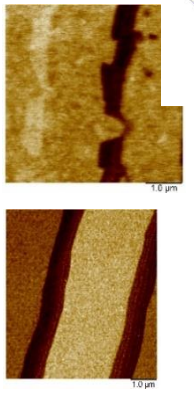
Project partners with UCL group for the first time directly observed how the antiphase domains originating at the Si/III-V material interface propagate through the device 3D structure, disrupting quantum wells order and electrically "shorting" the device. The methodology will guide CS engineers in finding solutions to eliminate this adverse phenomenon affecting novel optoelectronic components.
While the performance of III-nitride materials critically depends on their polarity, until now, the polarity could be assessed by the crude method of etching away the entire structure. For Sheffield GaN NWs, it was demonstrated that it is possible to not only non-destructively detect the polarity of the as-grown NWs, but also to observe the nanoscale domains of the opposite polarity within the individual NW. By probing key early stage of the III-nitride growth, it allows to guide manufacturing for best device performance.

Relevance to manufacturing

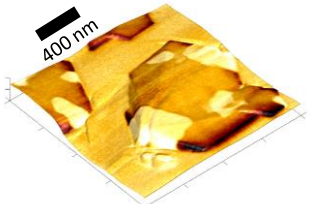
The project addresses the main thrust of the CS hub of successful combination of III-V devices with Si technology by providing solutions applicable to main CS manufacturing processes and structures. The novel methodology will provide a highly efficient platform to guide III-nitride on Si growth as currently all the planar III-nitride devices are of Ga-polarity, while nitrogen polarity demonstrates major advantages for both electronics and photonics. For III-V on various substrates, it will help to direct processes of defect free optoelectronics devices on the low cost Si substrates, and to optimise the performance of VCSEL optoelectronics structures. The comprehensive information provided by the novel methodology will boost the development of efficient III-V semiconductor lasers, solar cells and lighting sources while using low cost Si manufacturing technology.



Left image - 3D rendering of vertical cavity surface emitting laser (VCSEL) (Cardiff), colour - UFM nanomechanics. Right - surface potential map of the active VCSEL area showing different doping and multiple quantum well.



Left image - surface potential of GaA multiple quantum well structure showing disruption by APD domains. Right - structure without APD domair showing perfect electronic propertie of the optoelectronic device.



Nano-cross-section of the GaN NW showing the growth polarity via piezolectric properties map (colour)

Feasibility study:

Angled-Cage Etching of Semiconductors (ACES)

Lead applicant: Prof Robert Taylor, Oxford University
Partners: Seren Photonics, Cardiff University
Hub Mentor: Peter Smowton

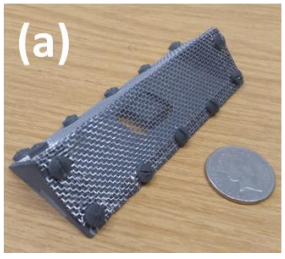
Summary

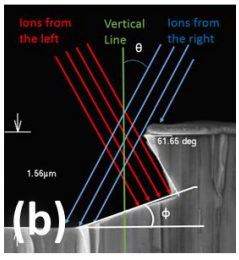
Gallium Nitride (GaN) is a wide bandgap semiconductor of huge economic importance, and the subject of the Nobel Prize for Physics in 2014. It is the base material for lasers in Blue-Ray drives, light emitting diodes in solid state lighting and can also offer improvements in performance of field effect transistors at high speed and high power. GaN is hard, inert and biocompatible. It can be alloyed with indium and aluminium to tune emission from 200 to 2000 nm, an unprecedented range for any semiconductor, making it a flexible platform for future device manufacturing. In addition, the material stiffness of GaN leads to high frequency and high-mechanical quality-factor oscillators that can be used as inertial sensors of superior performance to the silicon MEMS devices currently used in airbags, motion detectors and aerospace.

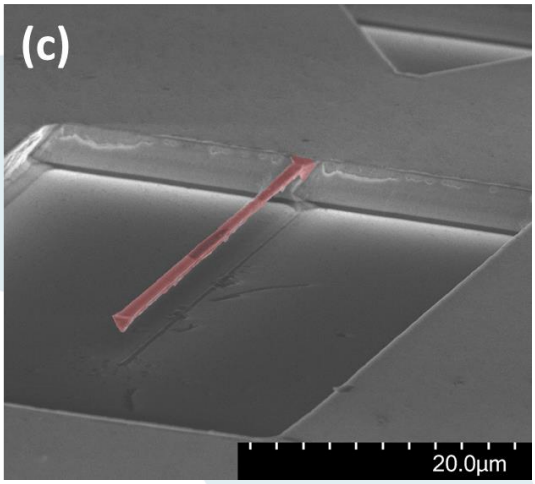
This feasibility study demonstrated that we can etch GaN at a steep angle using a novel single-step angled etch process with a Faraday cage. We created suspended GaN beams that guided light using the refractive Index difference between GaN and air. Our process can be used to manufacture integrated photonics devices, nanoscale lasers and sensors.

Outcomes/major findings

- Faraday cage can change the angle of
- etched sidewalls from +15º to -45º.
- Suspended waveguides and cantilevers
- can be manufactured in a single step.
- We have developed a design for a
- photonic crystal laser based on this
- process.







(a) a Faraday Cage used in the Feasibility Study (b) Cross-sectional SEM of an etched stripe, showing the characteristic shape, (c) suspended triangular cantilever 1µm wide and 35µm long.

Relevance to manufacturing

Faraday cage assisted etching allows us to control the etch angle, creating new functionalities.

We have pursued a “single step” etch process to reduce machine usage time.

* Cardiff University staff also funded by Ser Cymru I.

Feasibility study:

Solo – GaN 600V – 1.2kV Power Trench MOSFET

Lead applicant: Prof Petar Igic, Swansea University
Partners: CSC, SPTS, NWF, IQE
Hub Mentor: Phil Buckle

Summary

Gallium Nitride (GaN) vertical devices have the potential to enable new and highly efficient high voltage applications for a low carbon society such as electric vehicles. To date, a few research groups have reported on the successful fabrication of GaN vertical devices due to the considerable challenges associated with crystal growth, reliability and fabrication process. Exploiting a consortium made up of experts from the area of GaN material, simulation and fabrication, the goal of this team is to be amongst the first groups in Europe and the world to develop and push boundaries of what has been achieved in the field of GaN devices to date. Once quality benchmarked >600V critical processes are investigated and developed, i.e. p-epi on n-epi GaN growth and gate trench etch and dielectric deposition, they will form a solid platform for follow on project investigating the process modification to enhance the device's blocking capabilities and explore the areas not-to-date investigated in great details such as floating and biased p-bodies in GaN trenched devices and their effect on threshold and output instabilities.

Outcomes/major findings

We developed a low damage, low roughness vertical side-wall GaN etching process required for vertical devices (Figures 1a and 2).

We were also able to make advances in dielectric deposition, in the development of highly conformal Al_2O_3 high-k gate dielectric deposition process required to coat sidewalls of vertical device (Figure 1b).

We performed testing of dielectrics via fabrication of metal-insulator-metal capacitor test structures to investigate properties of high-k gate dielectrics. We demonstrated low leakage of high quality alumina layers (Figures 3 and 4).

In addition, we were able to demonstrate the feasibility of implementing trench etch and dielectric deposition modules for GaN vertical power devices.

Relevance to Manufacturing:

The proven feasibility of conformal dielectric deposition on vertical GaN sidewall is a critical step in the fabrication of vertical FET. We demonstrated highly controllable low leakage dielectric process with potential applications in a wide range of compound semiconductor projects.

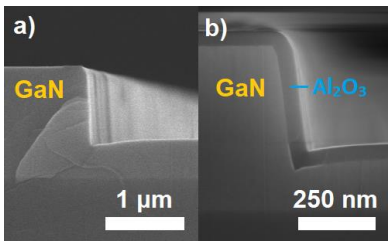


Figure 1 (a) Near vertical 1µm sidewall in GaN following etching. (b) Sidewall coated with alumina dielectric layer showing high conformality (thickness ~60nm).

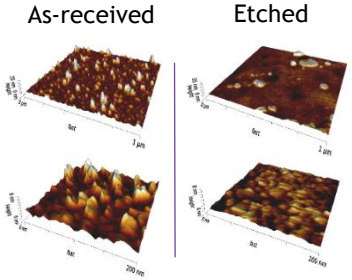


Figure 2. Atomic force microscope (AFM) scan of as-received and etched GaN surface showing reduction in roughness following etching. Scan size 2µm (top) and 200nm (bottom).

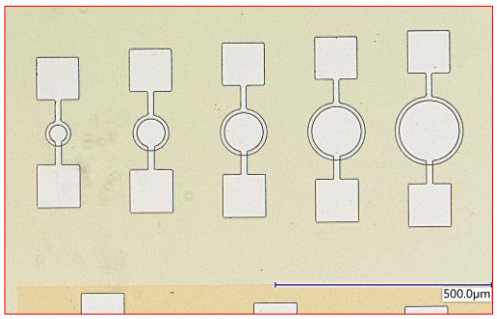


Figure 3. Microscope image of fabricated MIM capacitor test structure array for testing of high-k dielectrics. Contacts are Ti/Au on SiO2.

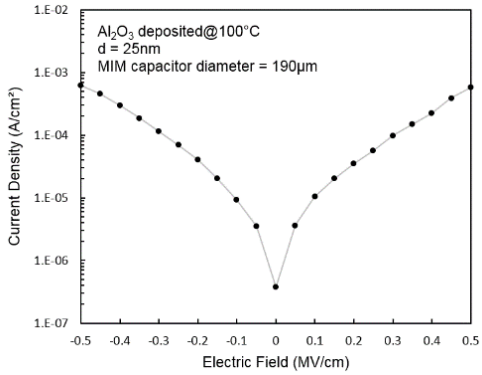


Figure 4. Microscope image of fabricated MIM capacitor test structure array for testing of high-k dielectrics. Contacts are Ti/Au on SiO2.

Feasibility study:

Feasibility of Compound Semiconductor Non-volatile RAM Manufacture on Si Substrates

Lead applicant: Prof Manus Hayne, Lancaster University
Partners: University of Warwick, IQE, Lancaster Material Analysis
Hub Mentor: Dave Wallis

Summary

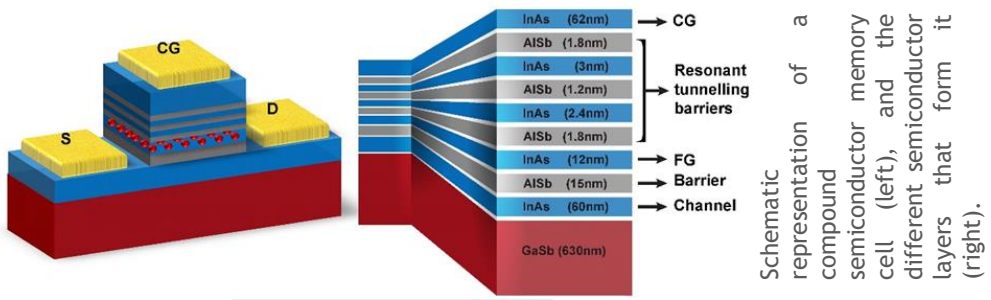
The technology behind the silicon-based processor and memory chips at the heart of all computers and electronic devices emerged in the 1970s. The memory chips, dynamic random access memory (DRAM), are fast, but volatile, meaning that information is lost unless it is refreshed multiple times per second. Furthermore, when data is read from DRAM it is destroyed (destructive read), and needs to be reprogrammed, which is inconvenient.
In this project we investigated the manufacturability of an innovative and completely new type of memory, one which fully exploits the opportunities for quantum design and engineering of materials and devices that are available in the compound semiconductor family. These memories are expected to be as fast as DRAM, but are non-volatile and with non-destructive read (NVRAM). Furthermore, despite this intrinsic robustness the energy needed to write or erase the data is substantially lower than for DRAM. Computers and electronic gadgets of the future using such memories would be fast, boot-free (instantly on or off) and consume significantly less power.

Outcomes/major findings

The focus of the study was the exploring the feasibility of implementing compound semiconductors on silicon by creating a 'virtual substrate' that is suitable for the memory devices. Achieving this is challenging because of the mismatch in crystalline lattices and the change from elemental (Si) to compound semiconductor. To tackle it, we took an approach that combined different layers of materials for the first time, growing gallium antimonide (GaSb) on gallium arsenide (GaAs) on germanium (Ge) on silicon (Si). A few iterations of this process were performed, guided by structural characterisation. Finally, a test layer of a key compound semiconductor used in the memory devices (indium arsenide, InAs) was grown on top, and its electrical properties tested. The results from the study were very promising, clearly demonstrating the feasibility of growing InAs and other compound semiconductors on Si wafers by this method.

Relevance to manufacturing

The development and commercialisation of a new memory technology is a gargantuan task. This is demonstrated by phase change memory, which was first explored in the 1960's, but has only very recently seen commercial success in the form of Intel's Optane. Lancaster's compound semiconductor memory has only been realised in single devices (bits) thus far. Manufacturing requires shrinking them to the nanoscale, exponentially increasing the number of bits on a chip, and implementation on industry-standard 300 mm Si wafers that are compatible with existing microelectronics chip production facilities.
This feasibility study was the first step on the road to manufacturability. The Si on Ge was grown by project partner IQE using a low-cost, mass-production method. We expect that, once optimised, the growth of all the other materials can be readily transferred to the production line.
The scaling down of device size and the scaling up of the number of bits, as well as further work on compound semiconductor growth, will require very substantial investment. However, the prospect of a compound semiconductor non-volatile RAM with such extraordinary properties is gripping. These are exciting times.



Schematic representation of a compound semiconductor memory cell (left), and the different semiconductor layers that form it (right).

Feasibility study

Spin Injection into Dilute Magnetic Gallium Nitride Transistors

Lead applicant: Associate Prof Karol Kalna, Swansea University
Partners: Cardiff University, CSC
Hub Mentor: Khaled Elgaid

Summary

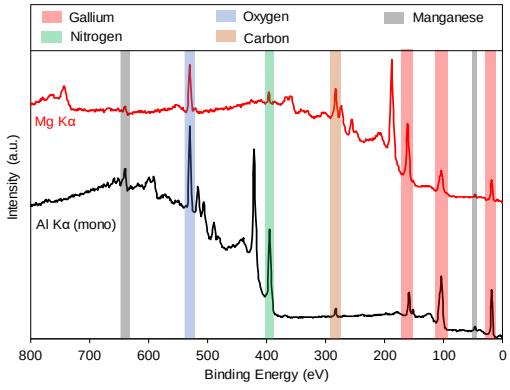
Spin semiconductor transistors are well recognised as potential future solutions for digital high-performance computation and memory. As Intel, Google, IBM and other companies are making major investments to build quantum computers, potential semiconductor spintronic transistors have become the object of strategic economic importance.
In this feasibility study, we have developed a doping methodology for gallium nitride (GaN) using manganese (Mn) to create spin-injecting contacts for wide-bandgap semiconductor transistors. We will use gallium manganese nitride (MnGaN), a dilute magnetic material with a low, 5% content of manganese to build a prototype of a contact for spin injection.

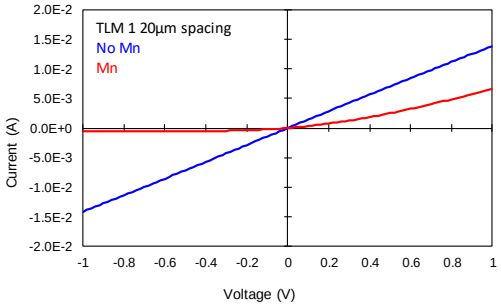
Outcomes/major findings

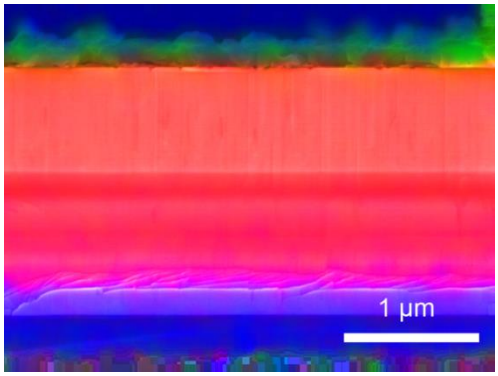
A diffusion of manganese using thermal annealing at 850ºC for 7h resulted in MnGaN with a Mn concentration of 4.5% as measured using XPS, very close to the desired concentration of 5% we aimed to achieve for the prototype.
Samples were characterised using a variety of techniques including XPS, SEM/EDX, magnetic AFM and TLM. Contacts using Mn were formed onto low-resistance ohmic contacts to make the TLM structures. The resulting contacts are Schottky forward bias current reduced by only 50% compared with ohmic contacts which allows spin-injection in AlGaN/GaN HEMTs.

Relevance to manufacturing

The outcomes of this feasibility study are essential in developing the technology strand of future wide-bandgap compound semiconductor spintronics technology for applications such as digital high-performance computation and memory.







Rectifying contacts formed following Mn doping of contact area. 50% reduction in forward bias current compared to ohmic I-V characteristics from a sample with no Mn
Contact resistance of 1 to 1.5 Ω.mm, can still be used for initial spin transport measurements.

Feasibility study:

New Characterisation Techniques for GaN RF Electronic Epitaxy

Lead applicant: Prof Martin Kuball, University of Bristol
Partners: Diamond Microwave Devices, IQE
Hub Mentor: Paul Tasker

Summary

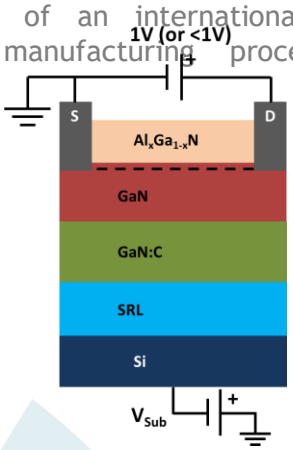
Compound Semiconductor gallium nitride (GaN) electronic devices used for monolithic microwave integrated circuit (MMIC) or discrete power applications require semi-insulating GaN epitaxial buffers which dramatically impact their performance in terms of important parameters such as short-channel effect, and current-collapse, as well as breakdown and leakage. In collaboration with industry, the Centre for Device Thermography and Reliability (CDTR) at Bristol University pioneered a new substrate ramp technique to characterise and optimise these GaN buffers. Working with IQE PLC and the Future CS Hub, the study concentrated on GaN-on-Si based epitaxy and scoped the feasibility of straightforwardly implementing this new approach in a manufacturing context. The study used "leaky dielectric" models of the epitaxial layers to understand trapping and leakage in the buffer. This is critically important for the establishment of an internationally competitive RF manufacturing process within the CSC.

Outcomes/major findings

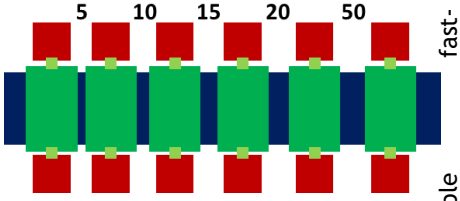
A fast and simple route for feedback to epitaxial growers without complete device fabrication was demonstrated using simple test structures. An example comparison was undertaken of two different epitaxial designs, with quite distinct trapping behaviour observed both across the wafers and between wafers. The results were used to qualitatively predict the impact of the epitaxy on final device RF efficiency and power density.
The approach and results were presented at the Reliability of Compound Semiconductors Workshop (ROCS 2019) in Minneapolis in April.

Relevance to manufacturing

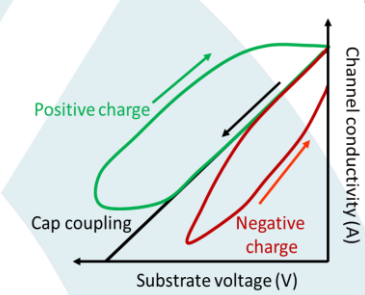
Traditionally radio frequency (RF) epitaxy can only be qualified by full device fabrication and test. The substrate ramp technique can provide feedback on material quality in a fraction of the time, dramatically shortening process development times, and vastly reducing the cost involved.



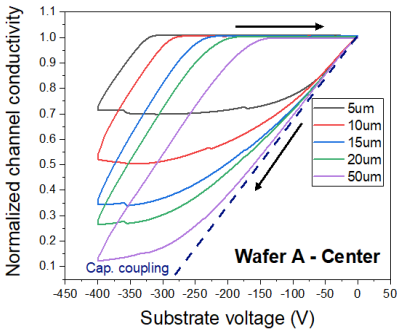
To test a GaN-on-Si epitaxial stack, a bi-directional voltage ramp is applied to the Si substrate and the conductivity of the channel is measured.



Simple fast-turnaround test structures fabricated at ICS.



Epitaxy conduction mechanisms and charging can be sensed using the channel conductivity.



Example data showing positive charging during the voltage ramp, and no remaining charge after the substrate voltage returns to zero. This is characteristic of good epitaxy.

Key performance indicators

Annual and long-term targets to measure success

The Future CS Hub has a number of targets formed of measurable research outputs that are carefully designed to measure the success of the Hub in the context of the CS research environment. Many of these targets are only possible to achieve in the long-term, while others can demonstrate more immediate success for the Hub.

The Key performance indicators for the Future CS Hub are detailed below.

Later in this report we will highlight some key achievements in the last year for the Hub, including new partners and research funding.

KPI	Success criteria
New industrial partners, based on exciting manufacturing challenges	5 per annum
New universities joining	5
Close collaborative links with other EPSRC Manufacturing Hubs and the EPSRC Centre for III-V Technology	Joint activities / events
Close collaborative links between the hub and major complementary overseas centres of excellence such as MIT, IMEC or NTU Singapore	2 over duration of Hub
Compound Semiconductor training centre activities to include: a) university and industry funded doctoral level training, b) MSc courses c) on-job and/or apprenticeship training to support industry d) summer schools for postdocs and PhD students	Delivery of a number of training activities per annum
Research and industrial awards per year for associated activity	Average of £5.5M (100% FEC) per annum
Conference presentations per year	Average of 10 per annum
Publications per year	Average of 20 per annum
Commercial impact activity to include: a) Number of IP disclosures/patents filed. b) Number of IP licences granted. c) Amount of VC funding generated, based on Hub technologies. d) New product roll-outs from partners, based upon Hub technologies. e) Sales value enabled by Hub technologies.	This is a late/lagging indicator and can be used later in the project to monitor success.
Outreach activity to include training	Delivery of a number of outreach activities per annum
Career development of Hub staff	Demonstration of staff development via securing fellowships, career training, etc.

The Year in Numbers

Based on our Key Performance Indicators, and some other important measures of success, we have generated some impressive numbers at the Future CS Hub.

34 Publications

80 Conference presentations & abstracts

32 Collaborations & partnerships

Including **26** new industrial partners and 6 new academic collaborators.

30 Further funding

Including new funding from Innovate UK and EPSRC, total £9,778,782

29 Outreach & engagement

Including activities from conference participation (at the inaugural Engineering Wales Conference, CoInnovate Conference, Institute of Physics engagement event and Wales Week in London CS Cluster Showcase and several others), providing work experience, providing bespoke communications training to **18** Hub affiliates.

12 Training activity

11 Awards & recognition

Consisting of **4** research prizes, and 7 invited conference presentations

7 Career development

Outreach

We have connected with high profile individuals at a number of events

Future CS Hub Director, Peter Smowton, and members of the team have been involved in some high profile outreach this year. In addition, Future CS Hub staff have attended several events, and an ongoing outreach plan is under development with Science Made Simple.

The Future CS Hub is committed to outreach, and we are very lucky to be able to work closely with Science Made Simple who are assisting us with a bespoke program of engagement and outreach, as well as training for Future CS Hub and associated staff. Training this year has focused on the development of engagement champions, and research demonstrators for use at public events.

Our Future CS Hub website continues to evolve with our flexible program of work: http:/compoundsemiconductorhub.org/

Our twitter feed has grown considerably this year to over 150 followers: @FutureCSHub

Our social media is being used regularly by our colleagues, for example, at the Institute for Compound Semiconductors (ICS), Ser Cymru Research Group and the GaN Centre (University of Sheffield) to advertise opportunities such as conferences, PhD studentships and Posts.

Over the next year, we plan to further develop our social media to include a Future CS Hub Facebook page.

Training forms part of our delivery program for outreach. We were able to provide Effective Networking training for 15 members of the Future CS Hub team via provider Will Kintish.

ICS clean room official opening: Increasing capability at Cardiff University

After significant investment from the EPSRC (Future CS Hub underpinning equipment award), Welsh Government and Cardiff University, the Institute for Compound Semiconductors underwent improvement, enhancing previous capabilities.

The ICS welcomed local business leaders to an event, opening the new facility and showcasing the solutions available for companies. The ICS is closely interlinked with the Future CS Hub in terms of facilities and collaboration.

Members of the Future CS Hub team attended the event as a networking opportunity, while Hub Director Peter Smowton led proceedings.

Economy Secretary Ken Skates commented: "*The ICS Clean Room is an outstanding example of a leading edge facility being developed with Welsh Government support. The project helps to bridge the gap between research and commercial solutions, taking ideas from the lab bench into our boardrooms and on to the shop floors of companies across Wales, so that the economic benefits are felt in communities across Wales. It is encouraging exactly the kind of cutting edge innovation and technology that Wales needs in order to compete globally and thrive.*"

UK Universities Minister visits ICS

The UK Universities and Science Minister, Chris Skidmore visited the facilities available at Cardiff University for compound semiconductor manufacturing research.

The Minister was introduced to recent improvements in the ICS facilities, as well as the complementary research of the Future CS Hub which is essential for developing the underpinning technologies for so many emerging megatrends

Other high profile visitors

The Future CS Hub was represented at other high profile visits by Director Peter Smowton.

These included a visit by a delegation from Chongqing Municipal Government (south western China) and the High Commissioner for India. Visitors were introduced to the Future CS Hub, ICS and the CS Catapult (by Andy Sellars), as well as the unique environment in South Wales which has allowed the successful development of the first CS Cluster.

Peter Smowton, Future CS Hub Director outlines the enhanced capability of the ICS clean room made possible in part by the Future CS Hub underpinning equipment award from EPSRC.

Future CS Hub staff and local business leaders networking at the ICS official opening event.

From left to right, Prof Colin Riordan, President and Vice-Chancellor, Cardiff University; Chris Skidmore, UK Minister for Science and Universities; Prof Peter Smowton, ICS and Future CS Hub director, Cardiff University.

Wales Week in London

Wales Festival of Innovation, with ESTnet as a key partner presented "CS Connected – Building the world's first compound semiconductor cluster" at an open event held on March 7th at Mary Ward House, London.

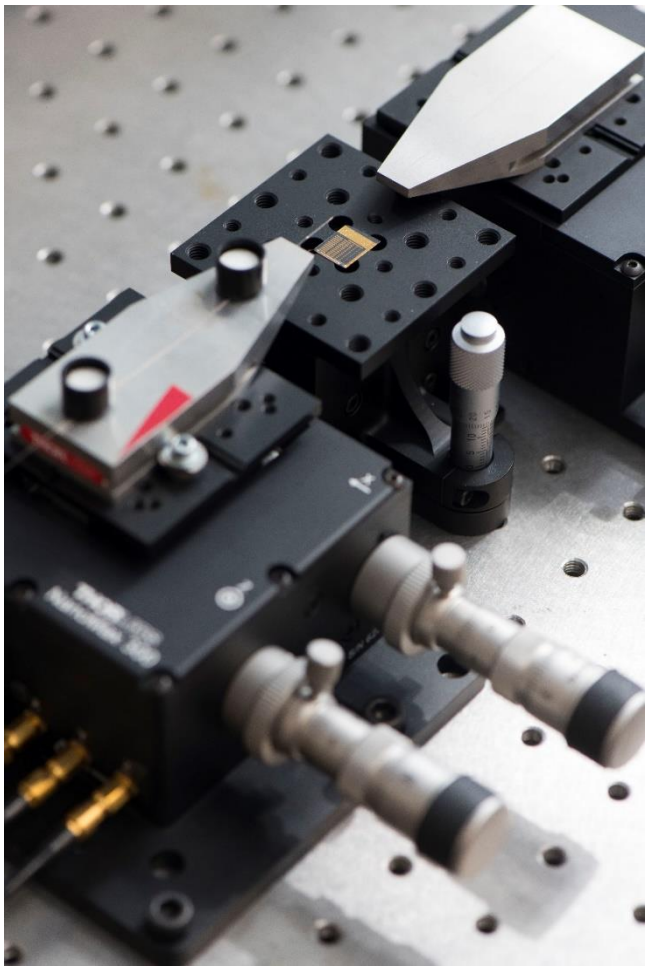
As part of CS Connected, the Future CS Hub was introduced to a varied audience of (around 80) academics, industrialists and laypeople.

The event included talks from Dr Phil Buckle (Future CS Hub and ICS), Dr Drew Nelson (IQE plc), Dr Wyn Meredith (CSC), Alastair McGibbon (CS Catapult), Chris Medows (IQE plc) and Sam Evans (Newport Wafer Fab).

The event was followed up with a reciprocal visit to Newport Wafer Fab where selected attendees (around 60) from industry and academia were invited to hear more detail about the CS Cluster, and tour the facilities at Newport Wafer Fab.

Phil Buckle, Work Package 2 lead representing the Future CS Hub at the reciprocal Wales Week in London event held at Newport Wafer Fab.

Representatives from each of the members of CS Connected before delivering their presentations to a mixed audience of academics and industrialists at Newport Wafer Fab.




OXFORD INSTRUMENTS
Process Chamber
11:41:44
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Base pressure reached
Load complete, wafer is in chamber
No Recipe Running
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Status
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Research output: Publications

Peer reviewed publications are a key indicator of our research success

Publications are a vital measure of success for the CS Hub, and we aim to develop as much high quality, unique and useful research as possible in the CS field. In last year's annual report, we were able to include 25 new publications for the CS Hub. This year we are able to report the publication of several new key research findings from all 4 original CS Hub academic partners (Cardiff University, the University of Manchester, the University of Sheffield and University College London).

CMOS-compatible multi-band plasmonic TE-pass polarizer. Abadia N, Ghulam Saber MD, Bello F *et al*. Optics Express. 2018:26(23);30292-30304

Physical modelling and experimental characterisation of InAlAs/InGaAs avalanche photodiode for 10 Gb/s data rates and higher. Abdulwahid OS, Sexton J, Kostakis I *et al*. IET Optoelectronics. 2018:12(1);5-10

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Strain Analysis of GaN HEMTs on (111) Silicon with Two Transitional AlxGa1−xN Layers. Cai Y, Zhu C, Jiu L *et al*. 2018:11(10);1968

Buffer induced current-collapse in GaN HEMTs on Highly Resistive Si Substrates. Chandrasekar H, Uren MJ, Eblabla A *et al*. IEEE Electron Device Letters. 2018:39(10);1556-1559

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Material and device characterization of Type-II InAs/GaSb superlattice infrared detectors. Delmas M, Debnath MC, Liang B & Huffaker D. Infrared Physics & Technology. 2018:94;286-290

Gain switching of monolithic 1.3 um InAs/GaAs quantum dot lasers on silicon. Hantschmann C, Vasil'ev PP, Chen S *et al*. Journal of Lightwave Technology. 2018:36(18);3837

O-band InAs/GaAs quantum dot laser monolithically integrated on exact (001) Si substrate. Li K, Liu Z, Tang M *et al*. Crystal Growth 2019. In Press. DOI: 10.1016/J.CRYSGRO.2019.01.016

Effect of rapid thermal annealing on threading dislocation density in III-V epilayers monolithically grown on Silicon. Li W, Chen S, Tang M *et al*. Journal of Applied Physics. 2018:123;215303

Low-noise 1.3 μm InAs/GaAs quantum dot laser monolithically grown on silicon. Liao M, Chen S, Liu Z *et al*. Photonics Research. 2018:6;1062-1066

III-V quantum-dot lasers monolithically grown on silicon. Liao M, Chen S, Park J *et al*. Semicond. Sci. Technol. 2018:33;123002

Electrically-Pumped Continuous-Wave Quantum-Dot Distributed Feedback Laser Array on Silicon. Wang Y, Chen S, Yu Y *et al*. Optica. 2018:5(5);528-533

Monolithic quantum-dot distributed feedback laser array on silicon. Wang Y, Chen S, Yu Y, *et al*. Optica. 2018:5;528-533

Research output: Conference presentations

Conference presentations and abstracts delivered by the Future CS Hub

Our researchers have been extremely proactive in delivering high quality, peer reviewed research. A great deal of this has been reported in conference publications, via invited talks, abstract presentations and keynote speeches. We are confident that in the following years, these conference outputs will translate into full publications wherever possible.

Increasing maximum gain in InAs quantum dot lasers on GaAs and Si. Shutts S, Spinnler C, Li Z *et al*. IEEE Photonics Conference (IPC), , Reston, Virginia, USA. 30th September – 4th October 2018. DOI: 10.1109/IPCon.2018.8527302

Growth of type-II InAs/GaSb superlattice. Delmas M, Rawal Y, Liang B & Huffaker D. SIOE Conference, Cardiff, Wales. 27th March, 2018

Material and device characterization of Type-II InAs/GaSb superlattice infrared detectors. Delmas M, Debnath MC, Liang B & Huffaker D. Quantum Structure Infrared Photodetectors Conference, Sweden. 17-21th June , 2018. DOI: 10.1016/j.infrared.2018.09.012

InGaAs-InP HBT-PIN Based Optoelectronic Integrated Circuit for over 10Gb/s Optical Systems. Muttlak SG, Sexton J & Missous M. SIOE Conference, Cardiff, Wales. 27th March 2018.

III-V quantum dot lasers epitaxially grown on Si. Chen S, Tang M, Wu J, Liao M, Seeds A & Liu H. Lasers and Electro-Optics/Pacific Rim. 31st July–4th August 2017.

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High-performance III-V quantum-dot lasers directly grown on silicon. Lui H. CIOP 2018, Beijing, China, 8 -11 July 2018.

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Research Highlight: CS Manufacturing (WP7)

3D Physical Magnetic Modelling and Device Simulations

Simulations play important roles in the compound semiconductor manufacturing process. Simulation contribute towards the understanding of the physical effects governing the compound semiconductor design process. Simulation can also provide important technical parameters for optimising the structures in order to fabricate efficient devices. With the advanced capabilities of material synthesis state-of-the-art compound semiconductor materials are evolving with new functionalities and are becoming more and more complicated in both their structures and their behaviours. The ultimate performance of devices fabricated from such materials relies on multiple variables, and a full understanding of their behaviour can be obtained through simulations using appropriate physical models. 3D device simulations using Finite Element Analysis (FEA) can predict the performances of devices fabricated from such advanced materials. This in turns help to construct prototype. Thus, simulations are cost effective and can provide insight into device operation and analysis of the underlying theoretical concepts. Data which are difficult to obtain from actual experiments can also be predicted using simulation.

Our compound semiconductor manufacturing and device fabricating facilities are well supported by a dedicated team of simulation experts. 3D Physical Modelling and 3D Finite Element Analysis (FEA) based simulation tools which include the software package SILVACO to perform 3D Physical Simulation, and CST Studio Suite/ COMSOL Multiphysics for FEA based 3D device simulations are used to perform these simulations. The team not only provides support to the on going research, but also perform exploratory works in order to seek out new and unexplored research opportunities.

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Research Highlight: MBE & Characterisation

Growth of III-V Compounds for electronic, optoelectronic and optical devices

In the last decades, demands for sophisticated device structures have increased markedly as a result of the rapid growth of electronic, optoelectronic and microwave industries. These demands are being met by increasingly complex thinner epitaxial structures grown from new materials using sophisticated techniques.

One of the successful techniques used in the CS Hub to fulfil the complexity requirement of modern epi-structures is Molecular Beam Epitaxy (MBE). In this technique, thermal atomic and/or molecular beams are generated in an ultra-high vacuum environment and their reaction with a heated substrate allows the epitaxial growth of high quality and high purity semiconductor crystal. The slow growth rate and the use of in-situ growth monitoring technique such as Reflection High Energy Electron Diffraction provides the ability to control material thickness and doping profile on an atomic scale.

At the University of Manchester, two epitaxy tools are available which are the V90H and V100HU dedicated to the growth of III-As and III-P compounds. The V100HU system is capable of handling 5x3" and 4x4" wafer platens. The research within the framework of the EPSRC in Future Compound Semiconductors Manufacturing Hub, is concentrated on the large scale manufacturability of novel, highly integrated 2D magnetic Quantum Well Hall Effect sensors for Non-Destructive Testing and Ultra high frequency RF circuits for emerging applications such as 5G wireless mobile communications, as well as ultra-high speed optical devices for the upcoming 10G and 25G fibre to the home and datacentres.

The epitaxial growth of complex III-V multilayers needs feedback to asses the integrity and consistency of the epitaxy to improve the layers electrical and optical quality. This is a key point in compound semiconductor manufacturing.
The optical and electrical properties of the epitaxial layers are evaluated routinely. Different characterization techniques are available in the EEE department of the University of Manchester including:

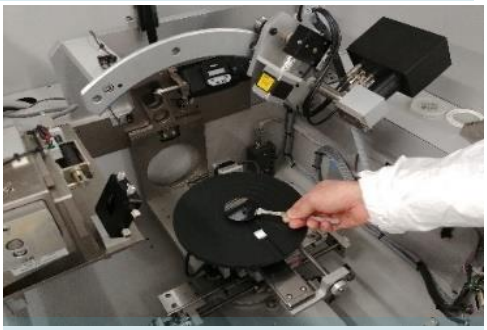
- ✓ High Resolution X-ray Diffractometer (Bede QC200 system). Bede RADS software is used for analysis
- ✓ Rapid Photoluminescence mapper (RPM2000) at room temperature.
- ✓ Hall Effect setup for the determination of mobility and carrier concentration
- ✓ Electrochemical CV profiling
- ✓ CV analyser and Mercury Probe Setup

RPM2000 PL system





Multi-wafer MBE reactor (V100)


Bede QC200 XRD system

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Research Highlight: Non-Destructive Testing

CS Manufacturing for industrial non-destructive testing applications

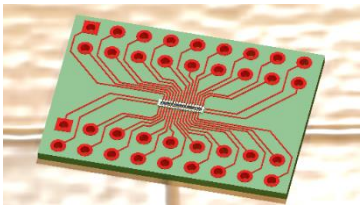
Fabrication of 2DEG Quantum Well Hall Effect sensor based devices to solve industrial problems.

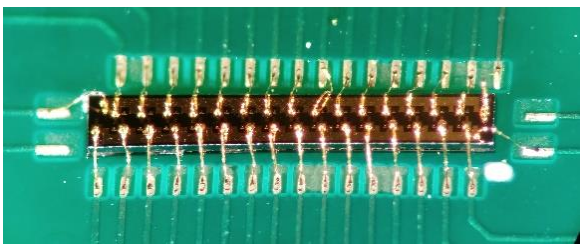
Recent developments in 2DEG-based Quantum Well Hall Effect (QWHE) sensors have generated interest and potential applications in a wide range of industries. In particular, the CS-HUB and the UK Non-Destructive Testing (NDT) community have funded the development of ultra-sensitive (nano Tesla range), ultra-low frequency (DC – 1 kHz) magnetometry and magnetovision systems. These interests arise mainly from the compound semiconductor sensors' versatility, inherently ultra high sensitivity of the 2DEG Hall sensors, the large bandwidth and high linearity coupled with the ability to integrate them into linear sensor arrays with micron scale pitch.

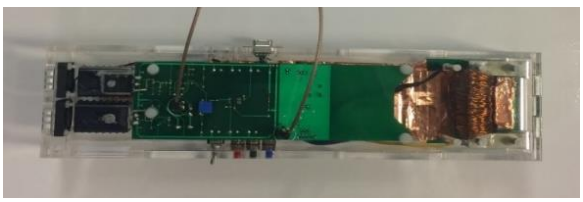
To date, these 2DEG Hall sensors have been used to explore the characterisation of materials based on their frequency-dependent magnetic properties, as well as detect surface-breaking discontinuities in manufactured components, including carbon steel welds. With the potential to design more sophisticated on-chip instrumentation amplifiers, superheterodyne current sources, filters and other circuitry, these 2DEG devices are leading the way in terms of bespoke fabrication for specific industrial applications such surface-breaking flaws in welds.

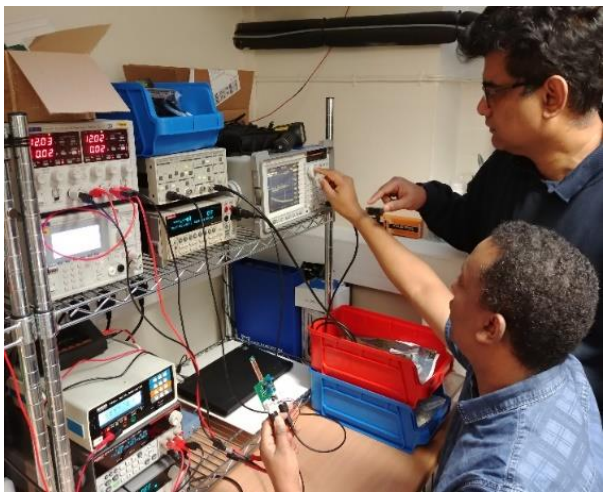
Successful development of QWHE sensor linear arrays with a fine pitch has been achieved, with potential applications including detecting surface-breaking flaws 10 μm in gape, magnetic domain imaging and subsequent microstructure analysis.

With continued support, the application of 2DEG QWHE sensors to solve industrial problems can be more extensively achieved, including using the behaviour of detected 3D magnetic field reconstruction/profiles of surface-breaking defects for asset monitoring, pre-failure mechanical stress detection and analysis.









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Research Highlight: Cleanroom Fabrication

Cleanroom fabrication for CS manufacturing

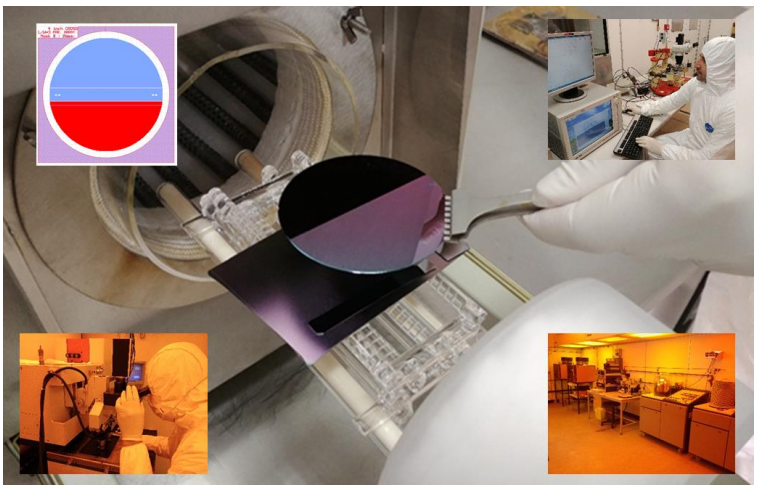
The fabrication of electronic, optoelectronic and optical devices.

Fabrication quality control is an essential element in manufacturing: in the production of any state-of-the-art CS device multiple individual tailored steps are necessary that can involve years of development. Each process requires two key ingredients to ensure a consistent fabrication. Firstly, the laboratory conditions where the devices are produced are strictly monitored, and secondly, the functionality of the devices are continuously evaluated and compared from run to run.

Large scale CS wafer fabrication commences only after successful small scale Research and development trials. These are essential to eliminate any fabrication related problems and minimise overall cost per device and maximise returns. The University of Manchester School of Electrical Engineering and electronics has dedicated class 1000 cleanrooms, process tools and test equipment that enable the production of multiple state-of-the-art processes. These laboratories have been operating for over two decades and are have enabled many Research and Development programs into full-wafer process (2, 3 and 4" wafer size).

The CS Hub is underpinning the operation and maintenance of these cleanrooms and testing tools to facilitate the production of full-wafer state-of-the-art devices. The laboratory is equipped with advanced i-line tools that are capable of processing small square tiles for research and development applications of full four inch wafers for manufacturing. Each process is uniquely defined and may require the use of one or more of these tools which have different operating costs. These include Laurell spinners, Karl Suss MA4 mask aligner, Oxford Instruments Reactive Ion Etcher, Kurt J Lesker PVD-75, Edwards (HHV) Auto 306 evaporators and multiple Agilent (Keysight) DC-IV Semiconductor Parameter analysers.

To date these laboratories have produced multiple high-speed devices including heterojunction bipolar transistors (HBT), Terahertz capable devices (Resonant Tunnelling Diodes), optical devices and magnetic sensors. The scaling up from Research and Development to full-wafer production has been successfully demonstrated for the magnetic sensors programme. The high yielding four-inch process developed provided individual elements for use in the magnetic camera designed at the University of Manchester. Arrays of elements have now also been designed and fabricated which will provide the means to detect domain wall motion at room temperature. If successful, scaling this R&D programme to full-wafer manufacturing will follow the same process route as the discrete magnetic sensors



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New award highlight: CSM CDT

Essential training in compound semiconductor manufacturing to be delivered by Future CS Hub academic partnership

In March 2018, EPSRC announced a new funding call for centres for doctoral training (CDT) to support students in undertaking a 4-year PhD, training the next generation of UK leaders for industry and research organisations as well as other areas.

The original 4 academic collaborators involved in the Future CS Hub, together with a number of existing and new industry partners, were successful in applying for a CDT in Compound Semiconductor Manufacturing (CSM). The first intake of post-graduate students into year one of the CSM CDT will happen in October 2019.

The CSM CDT will supply the UK with scientists and engineers with relevant skills, and importantly, a knowledge of the ecosystem of the entire supply chain in compound semiconductor manufacturing. This will be possible via unique access to the South Wales CS Cluster which spans all technology readiness levels.

Evidence suggests there is a critical skills shortage in this rapidly growing high technology sector. The CSM CDT will complement a wider training portfolio being implemented by the CS Cluster including apprenticeships and continued professional development activities designed to train and upskill the CS workforce.

A minimum cohort of 64 PhD students will receive training via the CSM CDT programme. Each student will be co-located with an academic and industry collaborator. Our current industry supporters number 24, and they have pledged a significant (>£3m) contribution to the CDT. We will continue to build new relationships with industry throughout the project to ensure that our students receive the best opportunities possible.

Students will be ideally placed to take advantage of recent major investment in compound semiconductor manufacturing including the EPSRC's underpinning equipment award for the Future CS Hub, as well as significant investment made by the Welsh Government and Cardiff University in the facilities and services available locally.

Taking advantage of the additional benefits of the CDT approach, students will benefit from a bespoke training plan, including organised training in transferrable skills such as project management and science communication.

For more information visit the CSM CDT webpage:
https://www.cardiff.ac.uk/study/postgraduate/research/programmes/programme/epsrc-cdt-in-compound-semiconductor-manufacturing

Or to make enquiries e-mail:
semiconductors-cdt@cardiff.ac.uk

Left: ICS Engineer, Dr Saleem Shabbir, loading a wafer onto an ellipsometer in the Institute for Compound Semiconductors (ICS) clean room, Cardiff University. The ellipsometer is part of the critical capital investment made by EPSRC in the facilities available for compound semiconductor manufacturing research at Cardiff University. Dr Shabbir is one of a team of ICS Engineers who provide a service to ICS users.
Below: Logos of the original academic partners to both the Future CS Hub and the CSM CDT.

CARDIFF UNIVERSITY
PRIFYSGOL CAERDYDD
UCL
The University Of Sheffield.
MANCHESTER 1824
The University of Manchester

New award highlight: Kairos

Laser manufacturability for miniature atomic clock applications

Named after the Greek god of time, the Kairos project aims to support the improved performance, including noise reduction, of the laser (vertical-cavity surface-emitting laser, VCSEL) while maintaining manufacturability for miniature atomic clock applications.

Following on from the successful Innovate UK / EPSRC co-funded project, MacV: Miniaturised atomic clocks using VCSEL pump sources, which focused on developing VCSEL specifications, we will continue to develop the technology involved for improved performance via the new Innovate UK funded Kairos project.

The new project brings together 9 industrial and academic partners from across the UK, with a strong track record in strategically relevant high technology fields.

The precise measurement of time is fundamental to the effective functioning of the services we take for granted in modern society. The Kairos project will develop a pre-production prototype of a miniature atomic clock for precise timing in a variety of essential services such as reliable energy supply, safe transport links, mobile communications, data networks and electronic financial transactions. Today, these services rely on GNSS for a timing signal which is easily disrupted either accidentally or maliciously. In prolonged GNSS unavailability these services stop functioning. The reliance on GNSS for precision timing, the consequent vulnerability of our essential services and the £5.2bn impact on the UK economy was made clear in a report from the London Economics in June 2017. That message is becoming widely understood and is creating a demand for timing solutions that are not GNSS dependent. The next generation miniature atomic clock arising from this project fills this need and will find widespread application in precision timing for mobile base stations, network servers for financial services, data centres, national power distribution networks and air traffic control systems. Further applications arise in areas where an independent timing reference is needed on a mobile platform and especially where no GNSS signal is available. A high performance compact clock would enable a range of useful capabilities. This project will address civil and military applications enabling a technical and economic success for the UK.

Essential components of the project for Cardiff University will include:

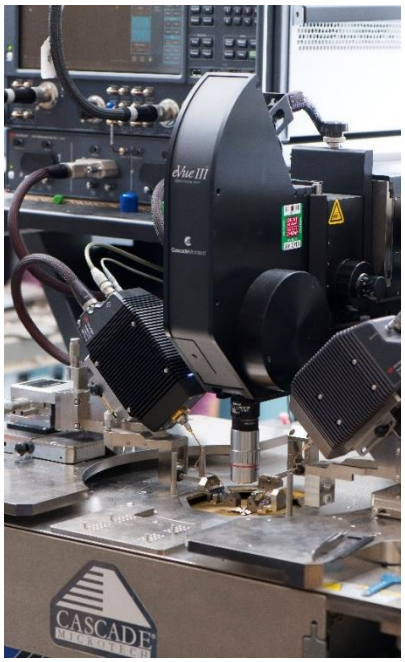
- Developing a well characterised stable and specific oxidation process
- Optimising VCSEL designs via modelling
- Characterising the VCSEL on-wafer to develop the design.

Expertise and equipment from the Future CS Hub will be essential for characterisation work on the Kairos project.

Kairos Partners

CSC
Cardiff University
ICS ltd
University of York
Teledyne e2v
National Physical Laboratory
Leonardo
Optocap Ltd
Altran

Innovate UK



Automatic probe station used to map the high frequency small-signal properties of devices on wafers up to 200 mm in diameter. The station can be configured to measure a variety of electronic and photonic devices, up to 130 GHz and 67 GHz respectively.

Contributors and staff

Work package leads and investigators

Prof Peter Smowton is Hub Director and Work Package 3 (Fast Fabrication) Lead, and Head of School at the School of Physics and Astronomy, Cardiff University

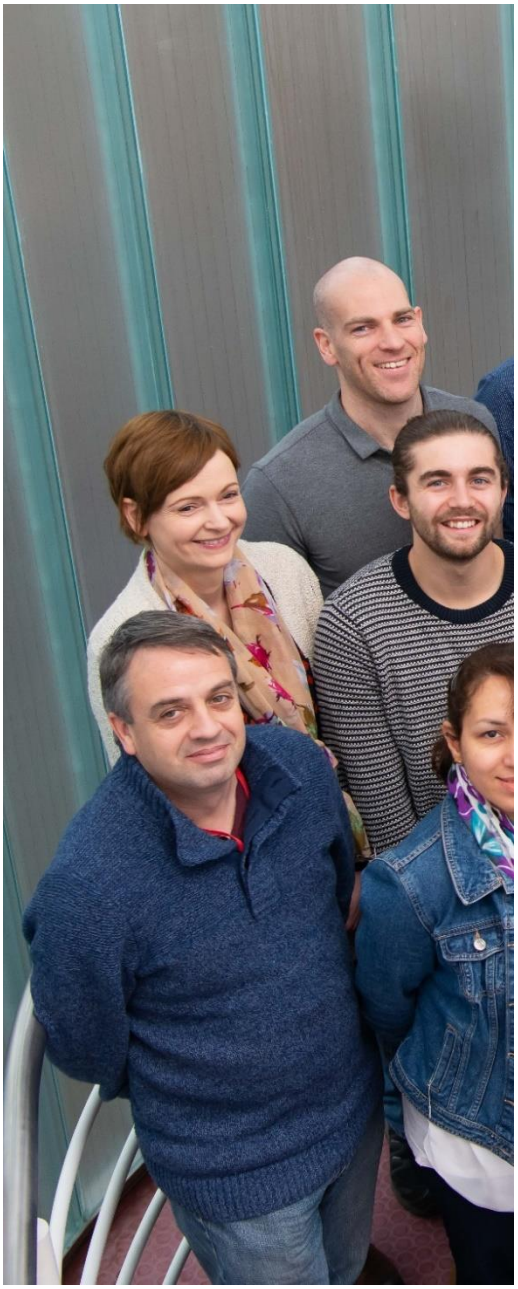
Prof Paul Tasker BSc, PhD, FIET, FIEEE FLSW is Grand Challenge 1 (The Connected Nation) Lead, School of Engineering, Cardiff University

Prof Diana Huffaker FIEEE, FOSA is Grand Challenge 2 (Sensors) Lead, Sêr Cymru Chair in Advanced Engineering and Materials, Science Director of the Institute of Compound Semiconductors at the School of Physics and Astronomy, Cardiff University

Prof David Wallis is Platform Work Package 1 (Epitaxy) Lead and Professor of Compound Semiconductors at the School of Engineering, Cardiff University

Dr Phil Buckle is Platform Work Package 2 (Fabrication) Lead and Reader at the School of Physics and Astronomy, Cardiff University

Prof Huiyun Liu PhD is Work Package 4 Lead (Optoelectronic devices for data comms) and Professor of Semiconductor Photonics at the Department of Electronic and Electrical Engineering, University College London



Prof Khaled Elgaid FIET, SIEEE is Work Package 5 Lead (RF Devices and MMICs) at the School of Engineering, Cardiff University

Prof Tao Wang BSc, MSc, PhD is Work Package 6 Lead (LEDs and RF diodes) and Professor of Advanced Optoelectronics at the Department of Electronic and Electrical Engineering, University of Sheffield

Prof Alwyn Seeds PhD, DSc (Eng), FREng, FIEE, FIEEE and Professor of Opto-Electronics at the Department of Electronic and Electrical Engineering, UCL

Prof Mo Missous, FREng is Work Package 7 Lead at the School of Electrical and Electronic Engineering, the University of Manchester

Dr Marie Delmas, PhD is Work Package 8 Lead and Marie Slodowska-Curie Fellow at the School of Physics and Astronomy, Cardiff University

Dr Nicolas Abadia is Work Package 9 Lead and Lecturer at the School of Physics and Astronomy, Cardiff University

Dr Max Migliorato is Senior Lecturer at the School of Electrical and Electronic Engineering, the University of Manchester

Prof Sir Michael Pepper, FREng, FRS is Pender Professor of Nanoelectronics at the Department of Electronic and Electrical Engineering, University College London

Dr Jiang Wu PhD is Lecturer at the Department of Electronic and Electrical Engineering, University College London

Dr Jon Willmot, PhD, MPhys is Lecturer at the Department of Electronic and Electrical Engineering, the University of Sheffield

Dr Rick Smith, PhD (EEE), BSc (hons) (Physics) is Lecturer at the Department of Electronic and Electrical Engineering, the University of Sheffield

Dr Qiang Li is Lecturer at the School of Physics and Astronomy, Cardiff University

Key associated and research staff

Dr Lewis Kastein
Dr Emmanuel le Boulbar
Dr Zhibo Li
Dr Chen Wei Liang
Clive Meaton
Dr Wyn Meredith
Dr Sudha Mokkapati
Dr Chris North
Dr Roberto Quaglia
Wendy Sadler MBE
Dr Majid Salhi
Dr Saleem Shabbir
Dr James Sexton
Dr Angela Sobiersierski

PhD students

Lydia Jarvis
Nicolas Poyiatzis
Ying Lu
Saad Muttlaak
Omar Abdulwahid
Tahani Albiladi
Ben Maglio
Curtis Hentschel
Fwoziah Albeladi
Dominic Kwan